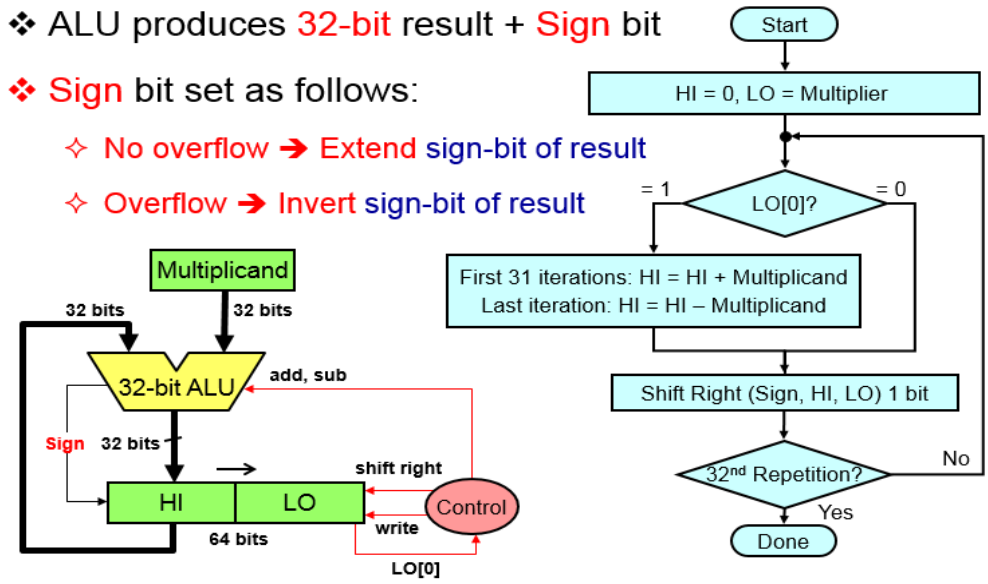
COE 405, Term 162

Design & Modeling of Digital Systems

Assignment# 4

Due date: Saturday, April 23

It is required to design an n-bit signed multiplier circuit. The architecture and the algorithm for performing signed multiplication are given below:



The example below illustrates the signed multiplication of two 4-bit numbers:

❖ Consider: 1010_2 (-6)×1111_2 (-1), Product=00000110_2 (+6)

❖ Check for overflow: No overflow ➔ Extend sign bit

❖ Last iteration: add 2's complement of Multiplicand

Iteration		Multiplicand	Sign	Product = HI, LO
0	Initialize (HI = 0, LO = Multiplier)	1 0 1 0		0 0 0 0 1 1 1 1
1	LO[0] = 1 => ADD		1	1 0 1 0 1 1 1 1
	Shift (Sign, HI, LO) right 1 bit	1 0 1 0		1 1 0 1 0 1 1 1
2	LO[0] = 1 => ADD		1	0 1 1 1 0 1 1 1
	Shift (Sign, HI, LO) right 1 bit	1 0 1 0		1 0 1 1 1 0 1 1
3	LO[0] = 1 => ADD		1	0 1 0 1 1 0 1 1
	Shift (Sign, HI, LO) right 1 bit	1 0 1 0		1 0 1 0 1 1 0 1
4	LO[0] = 1 => SUB (ADD 2's compl)	0 1 1 0	0	0 0 0 0 1 1 0 1
	Shift (Sign, HI, LO) right 1 bit			0 0 0 0 0 1 1 0

(i) Write a parametrizable Verilog module to model the signed multiplication circuit as a combinational circuit using for loop.

(ii) Write a test bench to test the correct functionality of your combinational signed multiplication circuit by instantiating a 4-bit multiplier and applying the following sets of inputs: -6*-1, -4*-3, -8*+7,+7*+7.

(iii) Implement your combinational signed multiplication circuit in FPGA and demonstrate its correct functionality. Include a video link that demonstrates the correct functionality of your implemented combinational signed multiplication circuit.

(iv) Next, consider implemting the signed multiplication algorithm as a sequential circuit. Show the design of the datapath components and their control signals.

(v) Derive the ASMD chart of the control unit that will control the operation of the signed multiplication circuit.

(vi) Model the data path of the sequential signed multiplication circuit in Verilog using a parametrizable module.

(vii) Model the control unit of the sequential signed multiplication circuit in Verilog based on your derived ASM chart in (v).

(viii) Write a test bench to test the correct functionality of your sequential signed multiplication circuit by instantiating a 4-bit multiplier and applying the following sets of inputs: -6*-1, -4*-3, -8*+7,+7*+7.

(ix) Implement your sequential signed multiplication circuit in FPGA and demonstrate its correct functionality. Include a video link that demonstrates the correct functionality of your implemented sequential signed multiplication circuit.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a PDF file that contains the following items:

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.