COE 405, Term 181

Design & Modeling of Digital Systems

Assignment# 3

Due date: Thursday, Oct. 25, 2018

Q.1. Consider the state table given below for a Mealy sequential circuit that computes the equation Z=3*X-4, where X is an unsigned number that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state.

Present State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
S0	S1	S2	0	1
S1	S2	S3	0	1
S2	S2	S4	1	0
S3	S3	S4	0	1
S4	S3	S5	1	0
S5	S4	S5	0	1

(i) Write a behavioral Verilog model for modeling your sequential circuit.

(ii) Write a Verilog test bench to test the correctness of your design for the following input values: {X=0}, {X=1}, {X=2} {X=3} and {X=4}.

(iii) Implement the sequential circuit on FPGA and demonstrate its correct functionality for the following input values: {X=0} and {X=3}. Include a link for a video demonstrating correct functionality.

Q.2. It is required to model a seconds counter that counts from 0 to 59. Assume that the counter has a synchronous Reset input that resets the counter to zero.

(i) Write a Verilog model for generating a 1 HZ clock.

(ii) Write a behavioral Verilog model for modeling an up/down module 60 counter that counts either up or down depending on a DIR input. When DIR=0, the counter will count up, otherwise it will count down. The counter will reset to 0 synchronously if a Reset input is pressed.

(iii) Implement the modulo-60 up/down counter on FPGA and demonstrate its correct functionality. Include a link for a video demonstrating correct functionality.