COE 405, Term 162

Design & Modeling of Digital Systems

Assignment# 2 Solution

Due date: Saturday, March 11

Q.1. Consider the given FSM that has 6 states, two inputs X and Y, and one output Z, represented by the following state table:

Present State	Next State				Output
	XY=00	XY=01	XY=10	XY=11	Z
S0	S1	S3	S0	S4	0
S1	S0	S4	S1	S5	0
S2	S2	S5	S0	S5	0
S3	S1	S3	S0	S4	1
S4	S0	S4	S2	S5	1
S5	S1	S3	S1	S3	1

(i) Determine the equivalent states.

S1	(3,4), (4,5)				
S2	(1,2), (3,5), (4,5)	(0,2), (4,5), (0,1)			
S3					
S4				(0,1), (0,2), (4,5)	
S5				(0,1), (3,4)	(0,1), (3,4), (1,2), (3,5)
	S0	S1	S2	S3	S4

Equivalent states are: (S0, S1, S2), (S3, S4, S5).

Thus, the machine can be reduced to two states: S0'=(S0, S1, S2), S1'=(S3, S4, S5).

(ii) Reduce the state table into the minimum number of states and show the reduced state table.

The reduced state table is:

Present State	Next State				Output
	XY=00	XY=01	XY=10	XY=11	Z
S0'	S0'	S1'	S0'	S1'	0
S1'	S0'	S1'	S0'	S1'	1

Q.2. Consider the given FSM that has 4 states, one input (X) and one output (Z), represented by the following state table:

Present State	Next State, Z	
	X=0	X=1
S0	S0, 1	S2, 0
S1	S0, 0	S2, 0
S2	S1, 0	S3, 0
S3	S1, 0	S3, 1

(i) Implement the FSM using the following state assignment: S0=00, S1=10, S2=01, S3=11.

	00	01	11	10
0	1 0	0 1	0 3	0 2
1	0 4	0 5	1 7	0 6

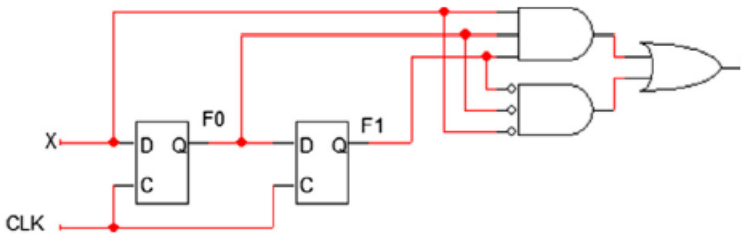
$Z = F1'\,F0'\,X' + F1\,F0\,X$

	00	01	11	10
0	0 0	1 1	1 3	0 2
1	0 4	1 5	1 7	0 6

$F0+ = X$

	00	01	11	10
0	0 0	0 1	1 3	1 2
1	0 4	0 5	1 7	1 6

$F1+ = F0$



(ii) Implement the FSM using the following state assignment: S0=10, S1=01, S2=11, S3=00.

	00	01	11	10
0	0 0	1 1	0 3	0 2
1	1 4	0 5	0 7	0 6

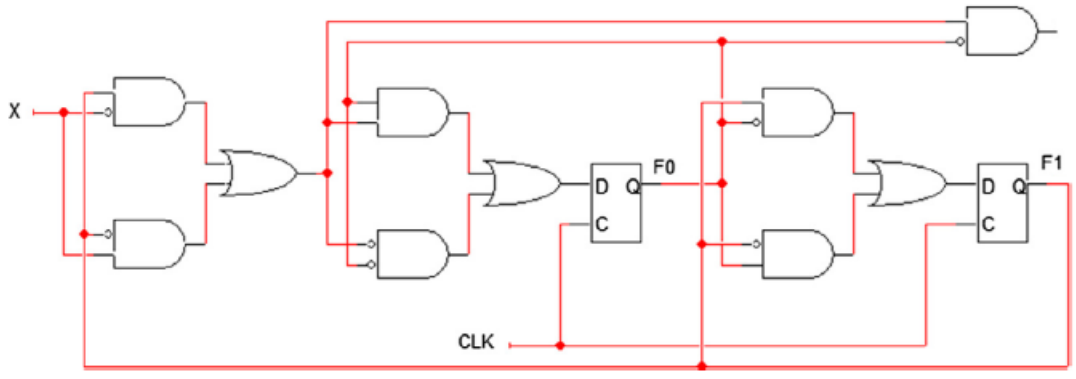
$Z = F1'\,F0'\,X + F1\,F0'\,X' = F0'\,(F1'\,X + F1\,X') = F0'\,(F1 \oplus X)$

	00	01	11	10
0	1 0	0 1	1 3	0 2
1	0 4	1 5	0 7	1 6

$F0+ = F1'\,F0'\,X' + F1'\,F0\,X + F1\,F0'\,X + F1\,F0\,X' = F1'\,(F0'\,X' + F0\,X) + F1\,(F0'\,X + F0\,X')$
$= F1 \oplus F0 \oplus X$

	00	01	11	10
0	0 0	0 1	1 3	1 2
1	1 4	1 5	0 7	0 6

$F1+ = F1'\,F0 + F1\,F0' = F1 \oplus F0$



(iii) Compare the area of the two resulting circuits.

The number of literals using the first state assignment is 6 while it is 14 using the second state assignment. We could also say that the first assignment uses an equivalent of 5 2-input primitive gates while the second state assignment uses 10 2-input primitive gates. Therefore, the first assignment produces a significantly lower area than the second assignment.

Q.3. It is required to design a sequential circuit using Mealy model that computes the equation Z=3*X-3, where X is an unsigned number that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state.

(i) Draw the state diagram for your sequential circuit. Make sure that your state machine is minimal and that it does not have any redundant state.

Present State	**Next State, Y**	
	X=0	**X=1**
S0 (B=3)	S1, 1	S3, 0
S1 (B=2)	S2, 0	S3, 1
S2 (B=1)	S2, 1	S4, 0
S3 (B=0)	S3, 0	S4, 1
S4 (C=1)	S3, 1	S5, 0
S5 (C=2)	S4, 0	S5, 1

(ii) Derive minimized equations for the output Z and next state variables.

Since we have 6 states, we need 3 FFs: F2, F1, and F0. We will use the following encoding: S0=000, S1=001, S2=010, S3=011, S4=100, and S5=101.

Transition Table:

Present State F2F1F0	**Next State, Y $F2^{+}F1^{+}F0^{+}$**	
	X=0	**X=1**
000	001, 1	011, 0
001	010, 0	011, 1
010	010, 1	100, 0
011	011, 0	100, 1
100	011, 1	101, 0
101	100, 0	101, 1

	00	**01**	**11**	**10**
00	1 0	0 1	1 3	0 2
01	1 4	0 5	1 7	0 6
11	?12	?13	?15	?14
10	1 8	0 9	111	010

$Y = (F0 \oplus X)'$

	00	01	11	10
00	1 0	1 1	1 3	0 2
01	0 4	0 5	0 7	1 6
11	?12	?13	?15	?14
10	1 8	1 9	111	010

F0+ = F1' F0' + F1' X + F1 F0 X' = F1' (F0' + X) + F1 F0 X' = F1 ⊕ (F0' + X)

	00	01	11	10
00	0 0	1 1	1 3	1 2
01	1 4	0 5	0 7	1 6
11	?12	?13	?15	?14
10	1 8	0 9	011	010

F1+ = F1 X' + F2' F1' F0 + F2' F1' X + F2 F0' X'

	00	01	11	10
00	0 0	0 1	0 3	0 2
01	0 4	1 5	1 7	0 6
11	?12	?13	?15	?14
10	0 8	1 9	111	110

F2+ = F2 X + F2 F0 + F1 X

(iii) Write a Verilog model for modeling your sequential circuit.

```
module Y3XM3 (output reg Z, input X, Reset, CLK);

        parameter S0 = 3'b000;//B=3
        parameter S1 = 3'b001;//B=2
        parameter S2 = 3'b010;//B=1
        parameter S3 = 3'b011;//B=0 & C=0
        parameter S4 = 3'b100;//C=1
        parameter S5 = 3'b101;//C=2

reg [2:0] CS, NS;

always @ (posedge CLK, posedge Reset)
begin
  if (Reset)
     CS <= S0;
```

```
  else
    CS <= NS;
end

always @ (X or CS)
begin
Z = 0;
case (CS)
S0:  if (X)  NS=S3;   else begin Z=1; NS=S1; end

S1: if (X) begin Z=1; NS=S3; end  else NS=S2;

S2:  if (X) NS=S4;  else begin Z=1; NS=S2; end

S3:  if (X) begin Z=1; NS=S4; end else NS=S3;

S4:  if (X) NS=S5;  else begin Z=1; NS=S3; end

S5:  if (X) begin Z=1; NS=S5; end else NS=S4;

default: begin Z='bx; NS='bx; end

endcase
end

endmodule
```

(iv) Write a Verilog test bench to test the correctness of your design for the following input values: {X=1}, {X=3}, {X=5} and {X=4}.

```
module Y3XM3_TB() ;

reg CLK, Reset, X ;
wire Z ;

Y3XM3 M1 (Z, X, Reset, CLK);

initial begin

CLK = 0 ; forever #10 CLK = ~ CLK ;

end


initial begin
```

```
//Applying X=1
@(negedge CLK) Reset=1;
@(negedge CLK) Reset=0; X=1;
@(negedge CLK) X=0;
@(negedge CLK) X=0;
@(negedge CLK) X=0;

//Applying X=3
@(negedge CLK) Reset=1;
@(negedge CLK) Reset=0; X=1;
@(negedge CLK) X=1;
@(negedge CLK) X=0;
@(negedge CLK) X=0;

//Applying X=5
@(negedge CLK) Reset=1;
@(negedge CLK) Reset=0; X=1;
@(negedge CLK) X=0;
@(negedge CLK) X=1;
@(negedge CLK) X=0;

//Applying X=4
@(negedge CLK) Reset=1;
@(negedge CLK) Reset=0; X=0;
@(negedge CLK) X=0;
@(negedge CLK) X=1;
@(negedge CLK) X=0;

end
endmodule
```

The simulation waveform below demonstrates the correct functionality of the designed sequential circuit: