COE 405, Term 181

Design & Modeling of Digital Systems

Assignment# 2

Due date: Saturday, Oct. 13

Q.1. Consider the given FSM that has 7 states, one input (X) and one output (Z), represented by the following state table:

Present State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
S0	S3	S1	0	1
S1	S3	S2	1	0
S2	S6	S5	0	1
S3	S0	S4	0	1
S4	S0	S5	1	0
S5	S1	S2	0	1
S6	S0	S2	1	0

(i) Determine the equivalent states.

(ii) Reduce the state table into minimum number of states and show the reduced state table.

Q.2. Consider the given FSM that has 5 states, one input (X) and one output (Z), represented by the following state table:

Present State	Next State, Z	
	X=0	X=1
S0	S1, 1	S2, 1
S1	S2, 0	S3, 0
S2	S2, 1	S3, 1
S3	S3, 0	S4, 0
S4	S3, 1	S4, 1

(i) Implement the FSM using the following state assignment: S0=000, S1=001, S2=100, S3=010 and S4=101.

(ii) Implement the FSM using the following state assignment: S0=010, S1=101, S2=111, S3=001 and S4=011.

(iii) Compare the area of the two resulting circuits.

Q.3. It is required to design a sequential circuit using Mealy model that computes the equation Z=3*X-4, where X is an unsigned number that will be fed serially. Assume that the circuit has an asynchronous Reset input that resets the machine to the reset state.

(i) Draw the state diagram for your sequential circuit. Make sure that your state machine is minimal and that it does not have any redundant state.

(ii) Derive minimized equations for the output Z and next state variables.

(iii) Write a structural Verilog model for modeling your sequential circuit.

(iv) Write a Verilog test bench to test the correctness of your design for the following input values: {X=0}, {X=1}, {X=2} {X=3} and {X=4}.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a PDF file that contains the following items:

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.