Introduction to Intel Core Duo Processor Architecture

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Presentation Outline

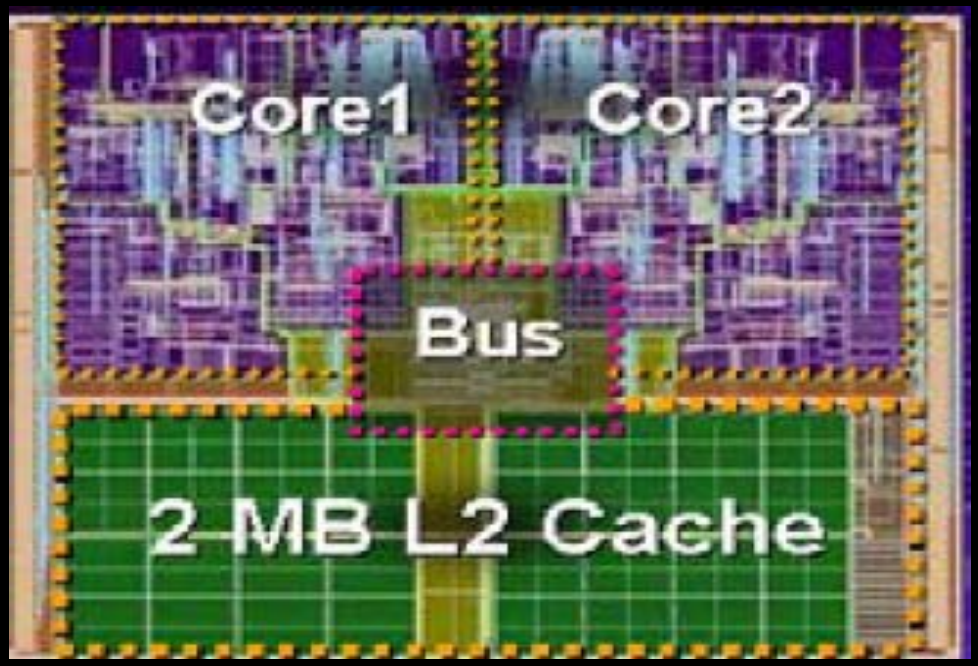
- BACKGROUND
- THE IMPROVED PENTIUM M PROCESSOR-BASED CORES
- CMP–GENERAL STRUCTURE
- POWER CONTROL
- INTEL Core SOLO PROCESSOR

BACKGROUND

- A member of Intel mobile processor
- First microarchitecture that uses CMP
- The target is:
  - Achieve high performance
  - Consuming low power
  - Fitting into different thermal envelopes.

BACKGROUND

- Intel Core Duo Inside
  - **Two Pentium M cores**
  - **Shared L2 cache**



BACKGROUND

- **performance and power targets :**
  - **Similar performance to the single thread performance processors**
  - **Improve in multithreaded and multi-processes software environments.**
  - **Same power consumption as previous generations of mobile processors**
  - **processor fits in all the different thermal envelopes the processor is targeted to**

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THE IMPROVED PENTIUM M PROCESSOR-BASED CORES

- **The main focus :**
  - **Support virtualization**
  - **Support the new Streaming SIMD Extension**
  - **Address performance inefficiencies**

THE IMPROVED PENTIUM M PROCESSOR-BASED CORES

- **Performance Improvements :**
  - **Streaming SIMD Extensions (SSE)**
  - **Floating Point**
  - **Integer**

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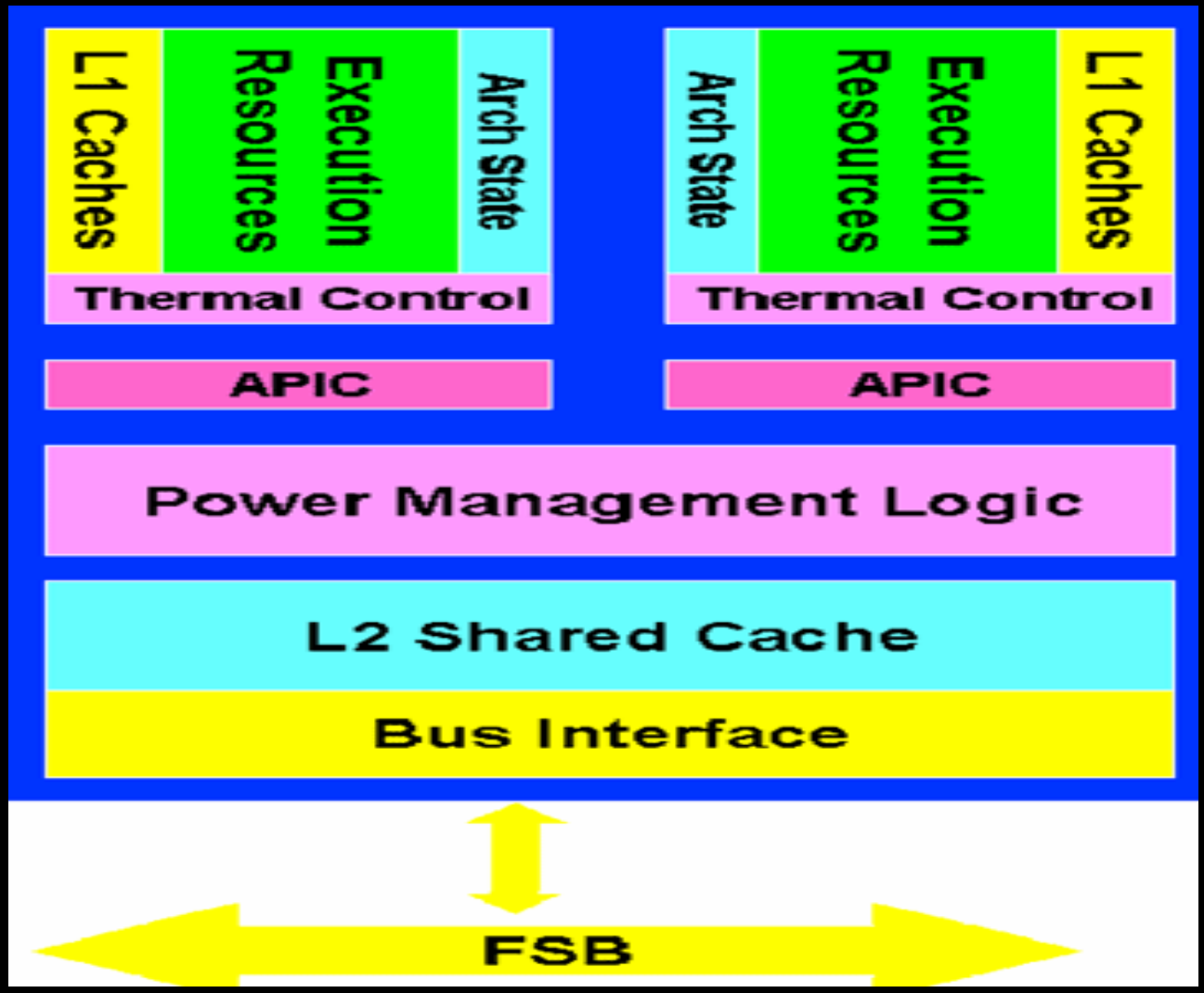
CMP–GENERAL STRUCTURE

- Independent APIC unit for each core
- The system behaves like DP system
- Compatible with Intel Pentium 4 processors
- Each core has an independent thermal control unit
- Power state together with package-level power state per-core

CMP–GENERAL STRUCTURE



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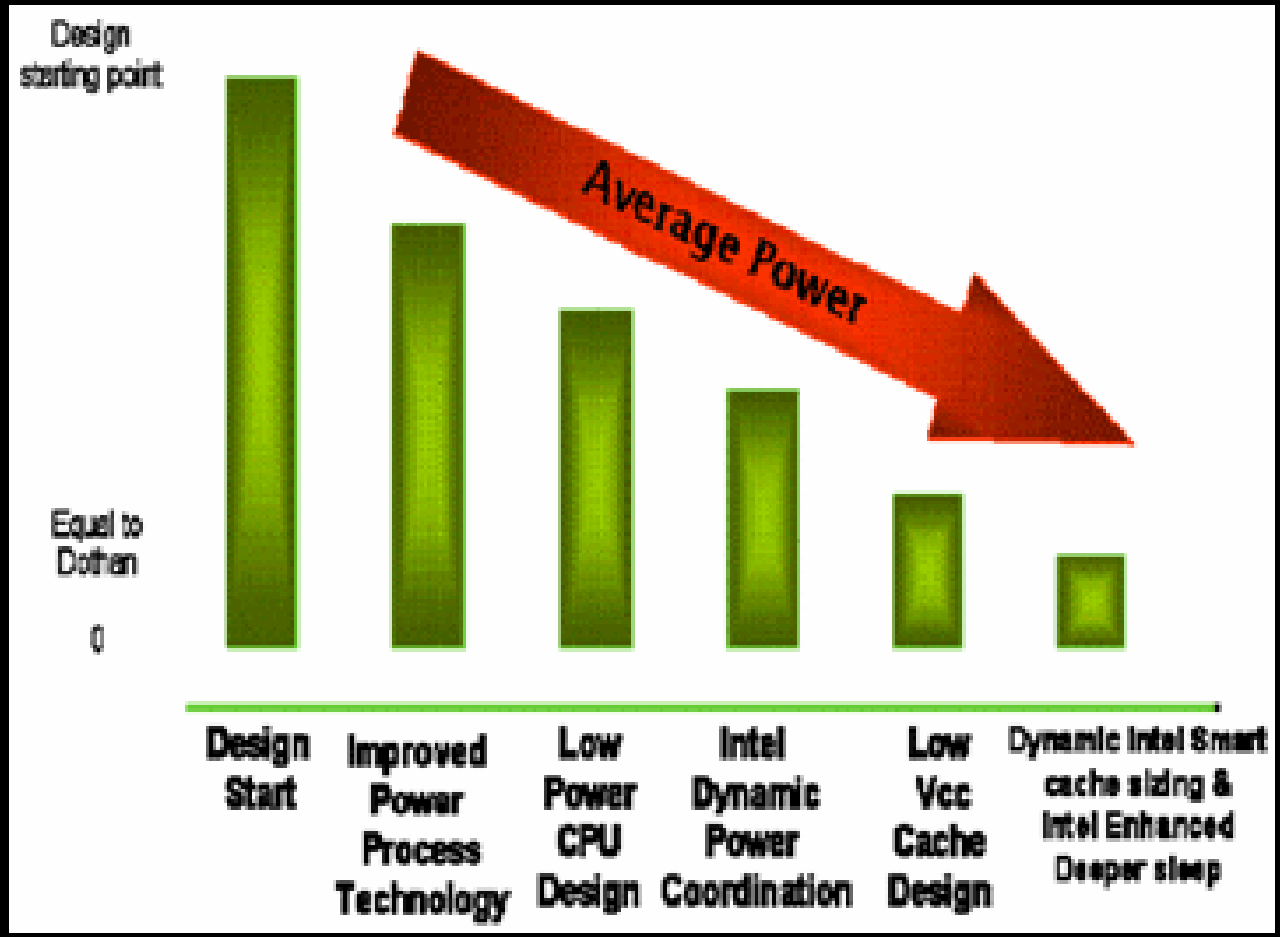
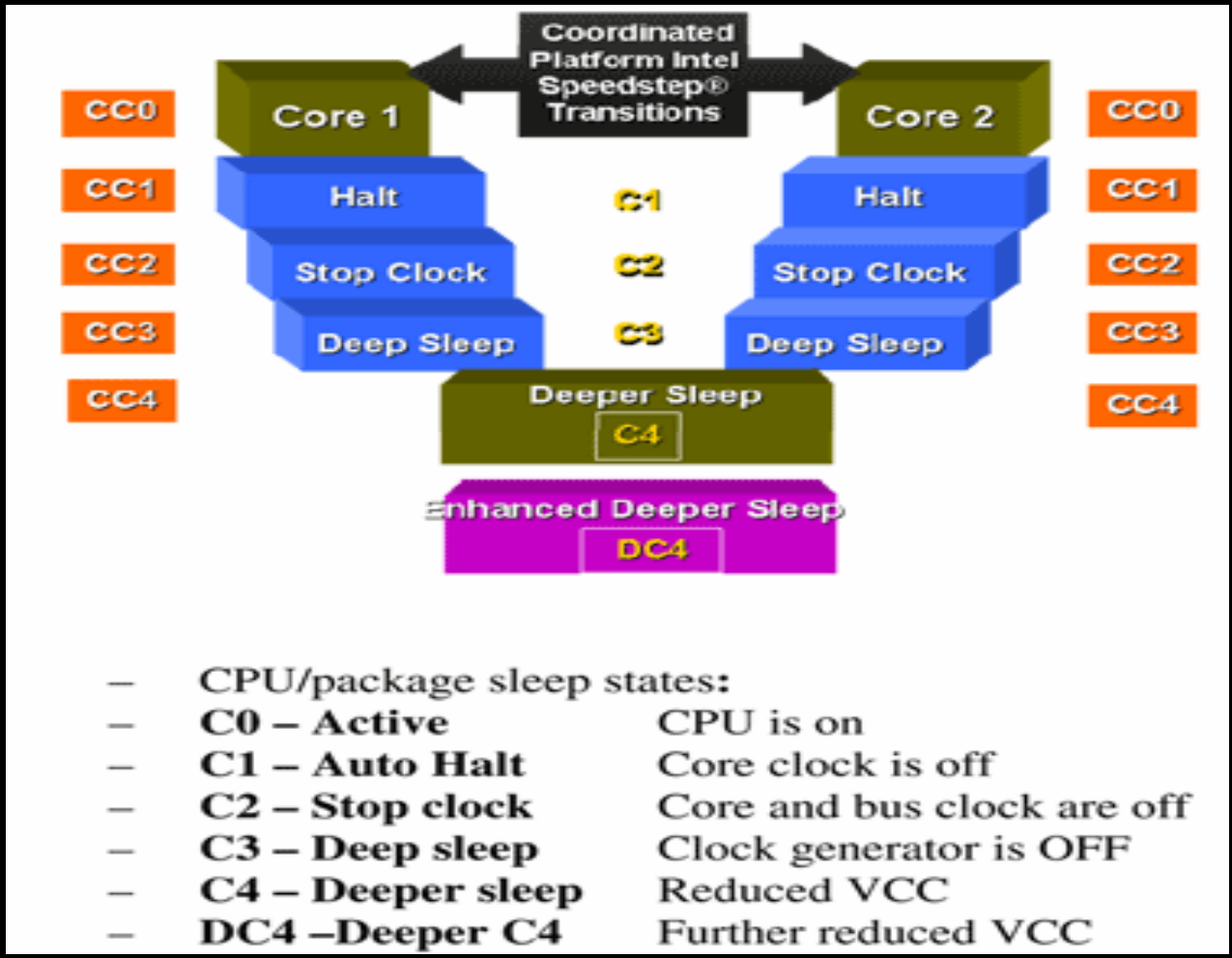
POWER CONTROL



POWER CONTROL

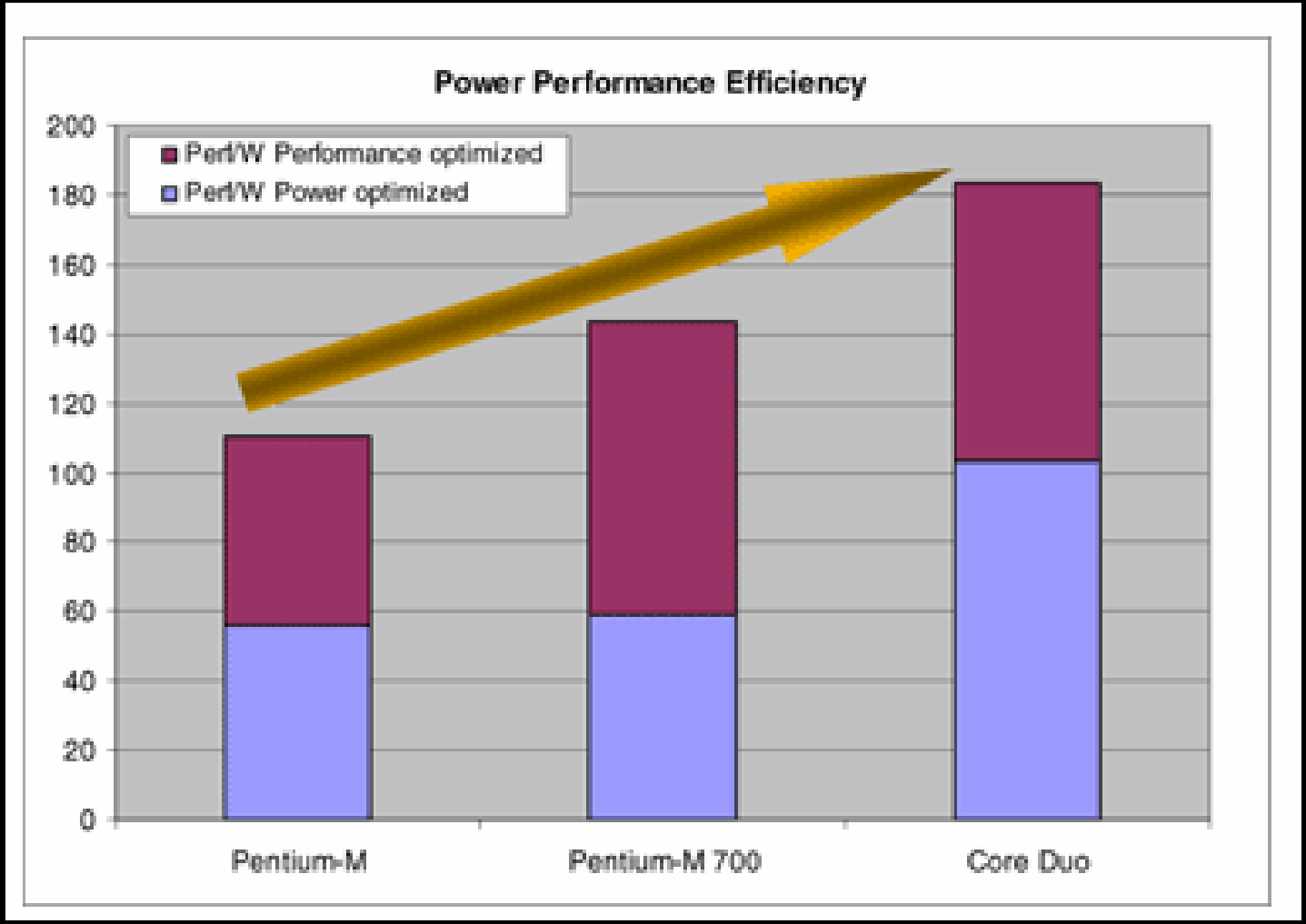
- **Tow main problems:**
  - **Same voltage and frequency**
  - **Same state at the same time**
- Per-core power state
- Synchronized power state

POWER CONTROL



- CPU/package sleep states:
- **C0 – Active** CPU is on
- **C1 – Auto Halt** Core clock is off
- **C2 – Stop clock** Core and bus clock are off
- **C3 – Deep sleep** Clock generator is OFF
- **C4 – Deeper sleep** Reduced VCC
- **DC4 –Deeper C4** Further reduced VCC

POWER CONTROL



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INTEL Core SOLO PROCESSOR

- Contains a single core only
  - Disabling one of the cores at the OS level as a BIOS option
  - Disabling one of the cores at the architecture level

CONCLUSION

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