Name: KEY Id#

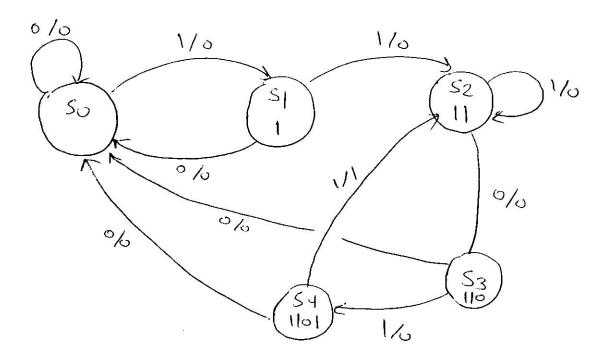
COE 202, Term 102 Fundamentals of Computer Engineering

Quiz#8

Date: Saturday, May 21, 2011

Q.1. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z. The output Z will be 1 when the circuit detects the sequence 11011 assuming overlapping sequence detection. Derive the state diagram for your circuit, and then obtain the circuit implementation optimizing the output and next state equations assuming D-FFs. Use binary code for state encodings. Assume the existence of a reset input to reset the machine to a reset state.

State Diagram:



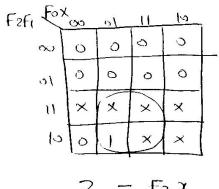
State Table:

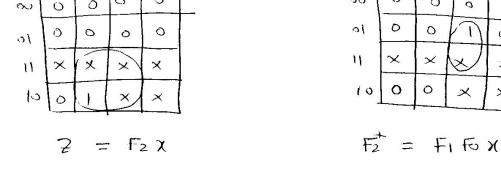
Current State	X	Next State	Z
S0	0	S0	0
S0	1	S 1	0
S 1	0	S0	0
S 1	1	S2	0
S2	0	S3	0
S2	1	S2	0
S3	0	S0	0
S3	1	S4	0
S4	0	S0	0
S4	1	S2	1

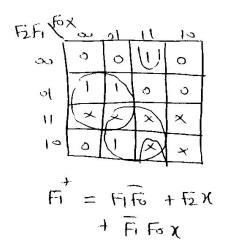
We assign the binary codes to the states and the state table becomes as follows:

Current State	X	Next State	Z
F2F1F0		F2F1F0	
000	0	000	0
000	1	001	0
001	0	000	0
001	1	010	0
010	0	011	0
010	1	010	0
011	0	000	0
011	1	100	0
100	0	000	0
100	1	010	1

K-map Simplification:







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Logic Works Circuit:

