## COE 202, Term 131

## Digital Logic Design

## Assignment\# 2 Solution

Due date: Thursday Nov. 28
Q.1. It is required to design a circuit that receives a 4-bit number $\mathbf{A}=\mathbf{A}_{\mathbf{3}} \mathbf{A}_{\mathbf{2}} \mathbf{A}_{\mathbf{1}} \mathbf{A}_{\mathbf{0}}$ and produces $\underline{7-}$ bit output $\mathbf{C}=\mathbf{C}_{7} \mathbf{C}_{6} \mathbf{C}_{5} \mathbf{C}_{\mathbf{4}} \mathbf{C}_{\mathbf{3}} \mathbf{C}_{\mathbf{2}} \mathbf{C}_{\mathbf{1}} \mathbf{C}_{\mathbf{0}}$. The circuit implements the following functions based on the values of the two selection inputs: S 1 and S 0 .

| S1 S0 | Function |
| :---: | :---: |
| 00 | $\mathrm{C}=2^{*} \mathrm{~A}$ |
| 01 | $\mathrm{C}=3 * \mathrm{~A}$ |
| 10 | $\mathrm{C}=4^{*} \mathrm{~A}$ |
| 11 | $\mathrm{C}=5^{*} \mathrm{~A}$ |

(i) Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed.

(ii) Model your design in logic works.

(iii) Test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness. For each function, test at least 2 input combinations of your choice to demonstrate correct functionality.



