## COE 202, Term 132

## Digital Logic Design

## Assignment\# 2

## Due date: Thursday April 17

Q.1. It is required to design a circuit that receives a 4-bit unsigned number $\mathbf{A}=\mathbf{A}_{3} \mathbf{A}_{\mathbf{2}} \mathbf{A}_{\mathbf{1}} \mathbf{A}_{\mathbf{0}}$ and produces $\mathbf{5}$-bit output $\mathbf{C}=\mathbf{C}_{5} \mathbf{C}_{4} \mathbf{C}_{3} \mathbf{C}_{\mathbf{2}} \mathbf{C}_{\mathbf{1}} \mathbf{C}_{\mathbf{0}}$. The circuit implements the following functions based on the values of the three selection inputs: $\mathrm{S} 1, \mathrm{~S} 1$ and S 0 .

| S2 S1 S0 | Function |
| :---: | :---: |
| 000 | $\mathrm{C}=\mathrm{A}+\mathrm{B}$ |
| 001 | $\mathrm{C}=\mathrm{A}-\mathrm{B}$ |
| 010 | $\mathrm{C}=2 * \mathrm{~A}$ |
| 011 | $\mathrm{C}=\mathrm{A}+1$ |
| 100 | $\mathrm{C}=\mathrm{A}-1$ |
| 101 | $\mathrm{C}=1$ if $\mathrm{A}==\mathrm{B}$ |
| 110 | $\mathrm{C}=1$ if $\mathrm{A}>\mathrm{B}$ |
| 111 | $\mathrm{C}=1$ if $\mathrm{A}<\mathrm{B}$ |

(i) Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed.
(ii) Model your design in logic works.
(iii) Test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness. For each function, test at least 2 input combinations of your choice to demonstrate correct functionality.

Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the circuits in one zipped file.

