Name: **Id#**

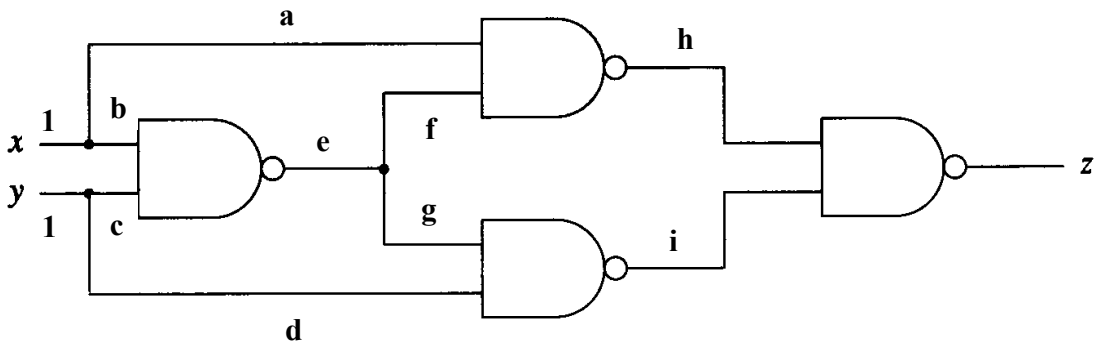
COE 464, Term 042

Testing of Digital Circuits

Quiz# 4

Date: Tuesday, March 29, 2005

Q1. Consider the circuit given below and assume that you have all the single stuck-at faults in the circuit, without fault collapsing, to be fault simulated under the test vector ***xy*= {11}**:



i. Logic simulate the circuit and mark the sensitive inputs of each gate with a •.

ii. Using **Critical Path Tracing** technique, determine the set of faults detected by the test vector ***xy* = {11}**. Write your solution in the table given below.

FFR Traced	Critical Lines	Stems_to_check	Stem Checked	Capture Line

Set of faults detected is: