COE 464, Term 042

Testing of Digital Circuits

HW#4

Due date: Sunday, May 8

Q.1. Consider the circuit shown in Figure 5.26(a) for a full-adder. Furthermore, consider the fault N s-a-0 in the circuit.

(i) Compute the controllability and observability costs for every line in the circuit using the generalized formulas (6.1) to (6.4).

(ii) Generate a test for the fault using the D algorithm. Use the costs computed in (i) to guide the selection. Show all the details of the algorithm.

(iii) Generate a test for the fault using the PODEM algorithm. Use the costs computed in (i) to guide the selection. Show all the details of the algorithm.

(iv) Generate a test for the fault using the FAN algorithm. Use the costs computed in (i) to guide the selection. Show all the details of the algorithm.

(v) Determine a lower bound on the detection probability of the fault based on signal probability computation. Compute this lower bound based on propagating the fault across the path *{N, N2, V, S}*.

(vi) Compute the exact fault detection probability by a random vector. Then, determine the length of the random sequence required to detect this fault based on the computed fault detection probability.

Q.2. Determine the primitive cubes and the propagation D-Cubes for an exclusive-OR module with three inputs.

Q.3. Consider the Combinational circuit c3540.bench with 50 primary inputs and 22 primary outputs. This circuit has a set of 3428 collapsed faults.

(i) Generate an 8000 random set of test vectors for this circuit and plot the fault coverage achieved versus the number of vectors applied.

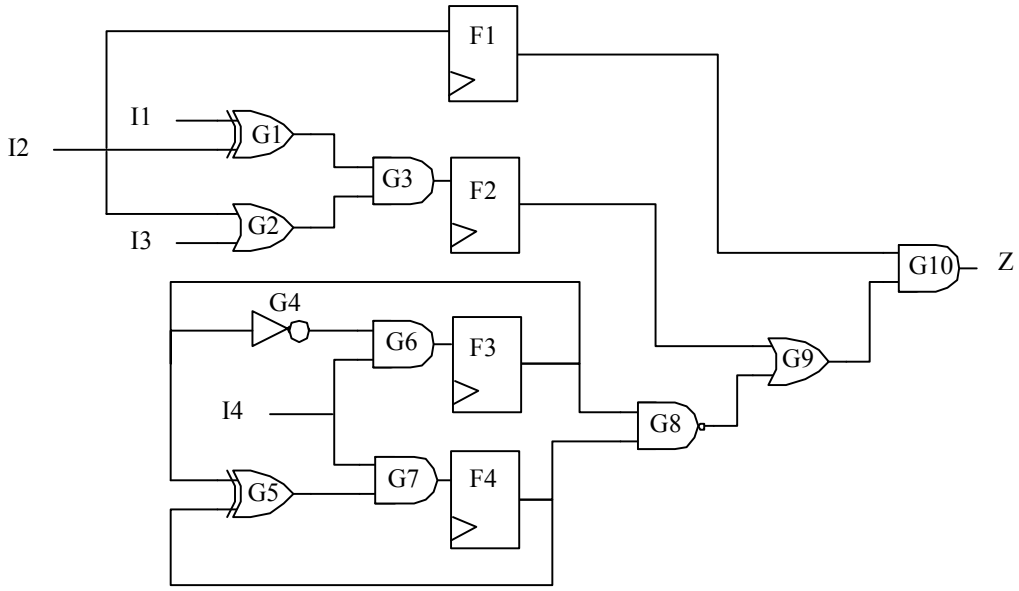
(ii) Eliminate the vectors that do not detect any fault, obtained from (i), and then plot the fault coverage achieved versus the number of vectors applied.

(iii) Use HITEC to generate deterministic patterns for this circuit. Run the algorithm for two iterations. Plot the fault coverage achieved versus the number of test vectors applied.

(iv) Compare the generated test sets in (ii) and (iii) in terms of fault coverage, test set length, and CPU time and comment on the results.

(v) Apply a two-phase approach where you apply 4000 random vectors first. Then, store the vectors randomly generated in c3540.vec. After that modify the TEST.run file generated by the command *do_hitec* to enable HITEC to fault simulate the vectors in c3540.vec before starting the ATPG process. Compare the test set generated using this approach to the ones generated in (ii) and (iii) in terms of fault coverage, test set length, and CPU time.

Q.4. Consider the sequential circuit shown below, which has four primary inputs, namely I1, I2, I3, I4, and one primary output, Z, and four D-FFs



(i) Generate a test sequence for the fault G3 stuck-at-1. Verify the correctness of the derived test sequence by fault simulating it using Proofs.

(ii) Generate a test sequence for the same fault using HITEC. Compare the obtained test sequence to what you obtained in (i).