COE 464, Term 042

Testing of Digital Circuits

HW#3

Due date: Sunday, April 17

Q.1. Consider the circuit shown in Figure 5.26(a) for a full-adder. Furthermore, consider the fault **N s-a-0** in the circuit.

(i) Generate a test for the fault using the **D algorithm**. Show all the details of the algorithm including the D-Frontier, the J-Frontier and the Decision tree. Whenever there are choices, select the choices in ascending alphabetical order. Verify your result by fault simulating the derived test using either PROOFS or HOPE.

(ii) Generate a test for the fault using the **PODEM algorithm**. Show all the details of the algorithm including the D-Frontier and the Decision tree. Whenever there are choices, select the choices in ascending alphabetical order. Verify your result by fault simulating the derived test using either PROOFS or HOPE.

(iii) Generate a test for this fault using HITEC and compare the obtained test to your solution.