COE 464, Term 042

Testing of Digital Circuits

HW#2

Due date: Tuesday, April 5

Q.1. Given a manufacturing process with a certain yield Y and a test with a certain fault coverage. Plot the Defect level (DL) curve as a function of the fault coverage for the cases when the yield Y=0.1, 0.2, 0.4, 0.6, 0.8, and 0.9 based on the following:

(i) Formula derived in class.

(ii) The Williams and Brown model: $DL=1-(Y)^{(1-d)}$, where d is the defect coverage of the test. Assume that d is equal to the fault coverage as an approximation. Compare the defect level curves in (i) and (ii).

Q.2. For the circuit shown in Figure 5.38, determine the faults detected by the each of the test vectors 101 and 010 based on each of the following methods, starting with a collapsed fault set based on fault equivalence. Show the details of each method.

(i) Deductive fault simulation.

(ii) Critical path tracing.

(iii) Verify your answer using the CPT implementation given in class using the following command: hope –t circuit.hope –C circuit.log –L 7 circuit.bench. Note that circuit.hope is the file containing the test vectors, circuit.log is the file that will contain the results, and circuit.bench is the file containing the circuit.

Q.3. Consider the full-scanned version of the circuit s5378f given as s5378f.bench. The number of collapsed faults in this circuit is 4603. The test set s5378f.vec detects 4563 faults, i.e. producing a fault coverage equal to 99.13%. Note that the remaining faults are redundant.

(i) Perform fault simulation of the test set on a randomly selected sample of *m* faults for each of the following values of *m: 50, 100, 500, and 1000*. Determine the fault coverage obtained, compare it to the exact fault coverage, and determine the error in each case.

(ii) Reverse the order of the test vectors in s5378f.vec. Then, fault simulate the reversed test set on all the faults and remove the vectors that no longer detect any fault. Comment on why this procedure can reduce the test set.

Q.4. Consider the circuits shown in Figure 5.38. Assume that the faults to be simulated are *d s-1-, e s-a-0, and b s-a-1.* Determine the expected number of detected faults and the detection probability for each fault for the test sequence T(a, b, c)={011, 000, 111, 101}. Perform fault simulation of the test set T and determine which of these faults are detected. Then, correlate the detection probability of each fault with its actual detectability status.