Name: **Id#**

COE 205, Term 092

Computer Organization & Assembly Programming

Quiz# 7

Date: Wednesday, June 9, 2010

Q1. Assume that a CPU has **16 instructions** with an opcode of 4 bits, seven **16-bit** general purpose registers namely AX, BX, CX, DX, SI, DI and SP, a **16-bit data bus**, and a **16-bit address bus**. Assume that all the instructions are 16-bit. The CPU has an **Arithmetic and Logic Unit (ALU)** with inputs A and B and output C, that can perform any of the following functions shown below based on the three selection lines AS2, AS1, and AS0:

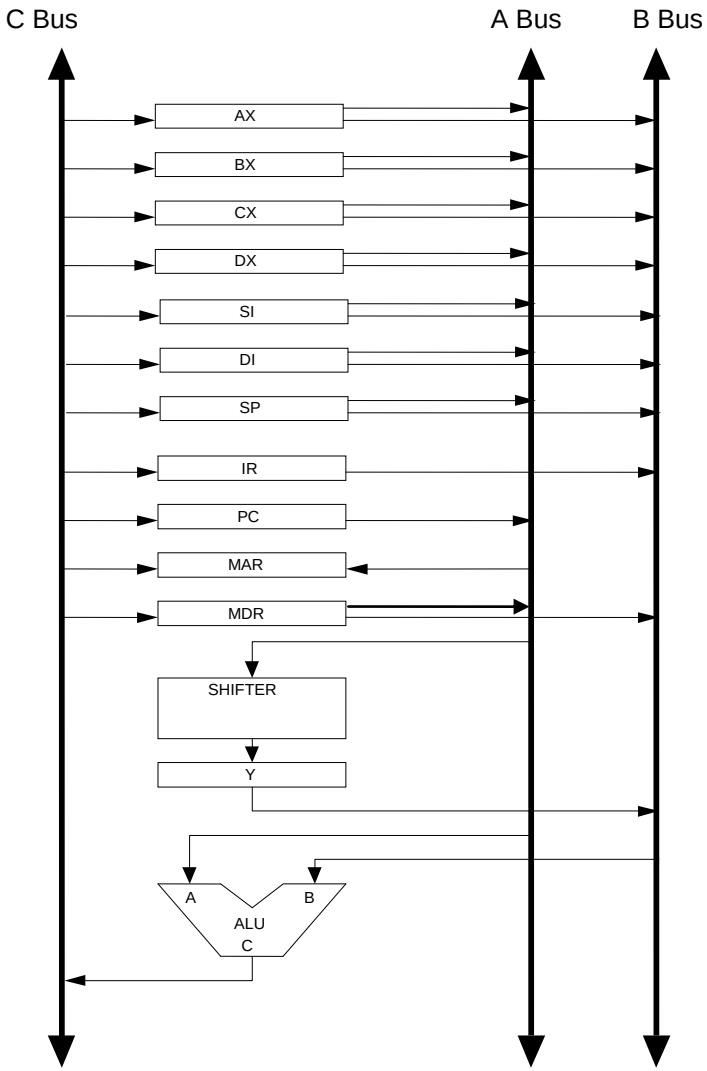
AS2 AS1 AS0	Operation
000	C=A+B
001	C=A-B
010	C=A+1
011	C=A-1
100	C=B
101	C=A+2
110	C=A-2
111	C=NOT A

The CPU has also a **Shift Unit** that can perform single bit shift as shown below based on the two selection lines SS1 and SS0:

SS1 SS0	Operation
00	No shift
01	Shift logic right
10	Shift logic left
11	Shift arithmetic right

Assume that the IR, PC, MAR, and MDR registers are also **16-bit registers**. Also assume that the instructions for this processor follow the syntax and semantics and addressing modes of the 8086 processor. Also assume that registers play the same role as assumed in the 8086 processor.

Assume that the data path of this processor is implemented using a **three-bus architecture** as shown in the next page.



Data Path Design

(i) Write the minimum number of control steps required for fetching an instruction from memory.

(ii) Write the minimum number of control steps required for the execution of each of the following instructions:

a. **MOV AX, [BX]** ; (Move the content of the memory operand pointed by register BX into register AX).

b. **XCHG AX, BX** ; (Exchange the content of registers AX and BX).

c. **PUSH AX** ; (Push the content of register AX on the stack).

d. **SAR SI, 1** ; Shift arithmetic right register SI by 1 bit.