

Name: KEY

Id#

COE 205, Term 082

Computer Organization & Assembly Programming  
Quiz# 6

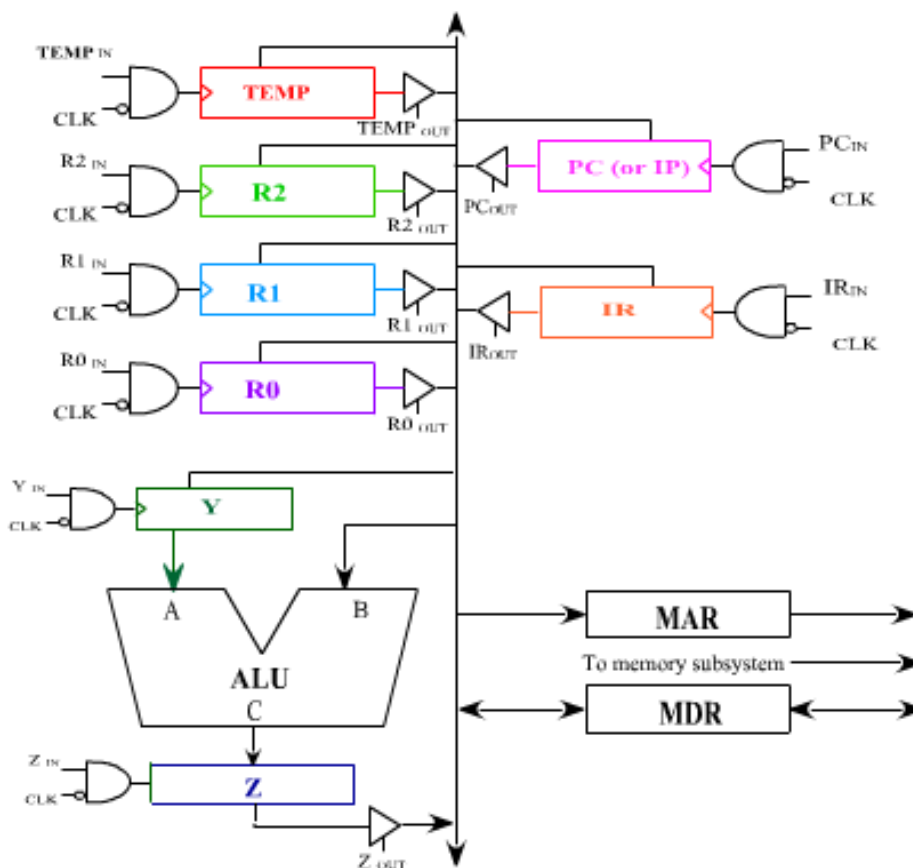
**Q1.** Consider the one-bus CPU organization shown below. Assume that the CPU has only three general registers, namely R0, R1, and R2 and it has also a temporary register Temp. Furthermore, assume that the ALU can perform any of the following four functions based on the control signals  $f1$ ,  $f2$ ,  $f3$ , and  $f4$ , as shown below:

$f1: C=A+B;$

$f2: C=A-B;$

$f3: C=A+1;$

$f4: C=A-1;$



(i) T<sub>1</sub> PC<sub>out</sub>, MAR<sub>in</sub>, Read, Yin  
 T<sub>2</sub> f<sub>3</sub>, Z<sub>in</sub>  
 T<sub>3</sub> Z<sub>out</sub>, PC<sub>in</sub>, WMFC  
 T<sub>4</sub> MDR<sub>out</sub>, IR<sub>in</sub>

(ii) a. JE label

T<sub>5</sub> PC<sub>out</sub>, Yin, if (ZF=0) END  
 T<sub>6</sub> IR<sub>out</sub>, f<sub>1</sub>, Z<sub>in</sub>  
 T<sub>7</sub> Z<sub>out</sub>, PC<sub>in</sub>, END

b. SUB J, 5

T<sub>5</sub> IR<sub>out</sub>, MAR<sub>in</sub>, Read, WMFC  
 T<sub>6</sub> MDR<sub>out</sub>, Yin  
 T<sub>7</sub> IR<sub>out</sub>, f<sub>2</sub>, Z<sub>in</sub>  
 T<sub>8</sub> Z<sub>out</sub>, MDR<sub>in</sub>, Write, WMFC  
 T<sub>9</sub> END

c. XCHG R1, R2

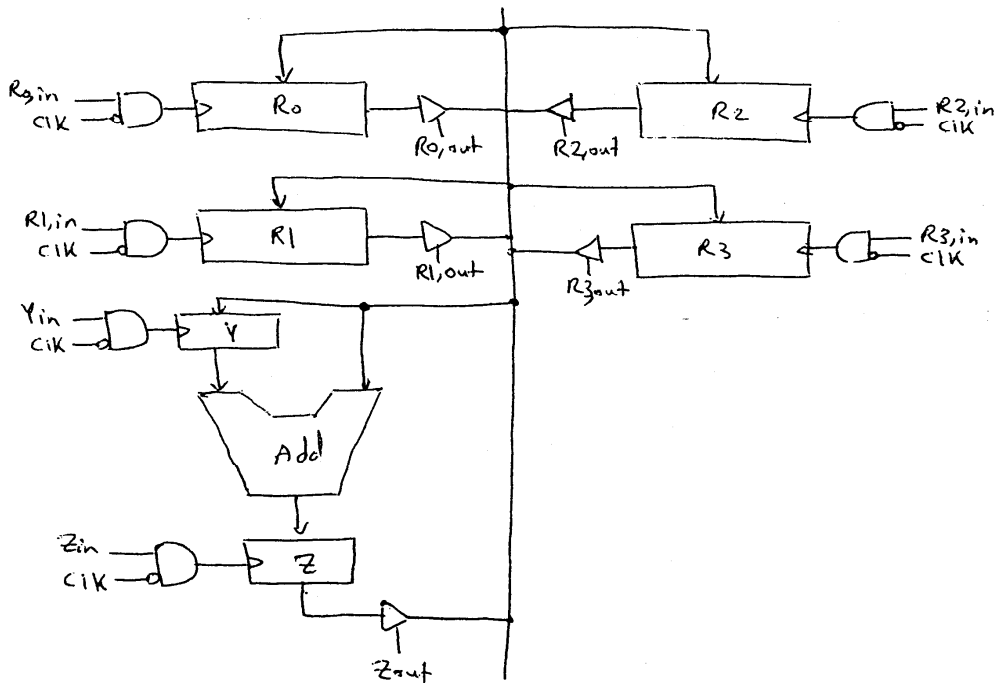
T<sub>5</sub> R<sub>1out</sub>, Temp<sub>in</sub>  
 T<sub>6</sub> ~~R<sub>2out</sub>~~, R<sub>1in</sub>  
 T<sub>7</sub> Temp<sub>out</sub>, R<sub>2in</sub>, END

d. Loop label

T<sub>5</sub> R<sub>0out</sub>, Yin  
 T<sub>6</sub> f<sub>4</sub>, Z<sub>in</sub>  
 T<sub>7</sub> Z<sub>out</sub>, R<sub>0in</sub>, if (ZF=1) end  
 T<sub>8</sub> PC<sub>out</sub>, Yin  
 T<sub>9</sub> IR<sub>out</sub>, f<sub>1</sub>, Z<sub>in</sub>  
 T<sub>10</sub> Z<sub>out</sub>, PC<sub>in</sub>, end

(iii) PC<sub>in</sub> = T<sub>3</sub> + JE · T<sub>7</sub> + Loop · T<sub>10</sub>

Q2. It is required to design a data path to execute the following two types of instructions: *MOV Rdst, Rsrc* and *ADD Rdst, Rsrc*, where *Rsrc* and *Rdst* can be either R0, R1, R2, or R3. Show the data-path design and indicate all the signals needed to control it. Note that you only need to show the interconnection of the registers with the adder i.e., there is no need to show the PC, IR, MAR and MDR registers.



Note that the signals  $R_{0,out}$ ,  $R_{1,out}$ ,  $R_{2,out}$ , and  $R_{3,out}$  are derived from the signals  $R_{src,out}$ ,  $R_{dst,out}$  and the content of IR. Similarly, the signals  $R_{0,in}$ ,  $R_{1,in}$ ,  $R_{2,in}$ , and  $R_{3,in}$  are derived from the signal  $R_{dst,in}$  and the content of IR.