Name: KEY **Id#**

COE 205, Term 031

Computer Organization & Assembly Programming
Quiz# 6

Date: Sunday, Jan. 4, 2004

Q1. Consider the one-bus CPU organization shown below. Assume that the CPU has only three general registers, namely R0, R1, and R2. Furthermore, assume that the ALU can perform any of the following four functions based on the control signals *f1*, *f2*, *f3*, and *f4*, as shown below:

f1: C=A+B; *f2*: C=A-B; *f3*: C=A+1; *f4*: C=A-1;

(i) Write the minimum number of control steps required to **fetch** an instruction using this CPU. Assume that the memory is asynchronous and that each instruction occupies one memory location.

(ii) Write the minimum number of control steps required to **execute** each of the following instructions:

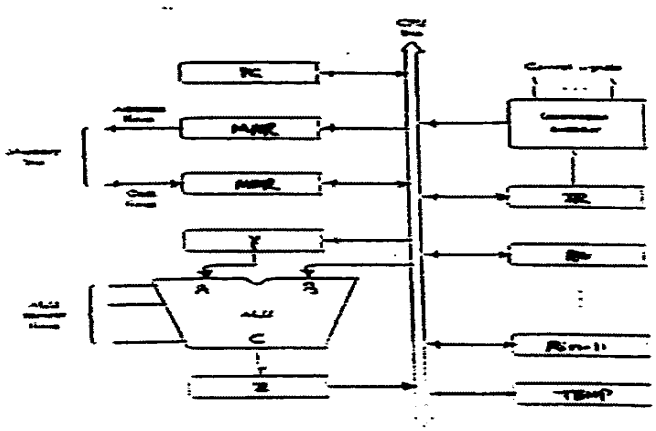
(a) JE label ; if the zero flag is 1, then jump to label. Assume that Label is a short address.

(b) SUB J, 5 ; subtract the constant 5 from the content of memory variable J.

(c) XCHG R1, R2 ; exchange the content of register R1 and register R2;

(d) LOOP label ; decrement the content of R0 and then branch conditionally to *label* if the zero flag equals to 0. The branch address is specified using relative addressing mode.

(iii) Assuming that the instruction set of the CPU consists of only the four instructions mentioned above, determine the logic needed in the encoder of a hardwired control unit for the signal PC_{in}.



(i) T_1 PCout, MARin, Read, Yin
T_2 f3, Zin
T_3 Zout, PCin, WMFC
T_4 MDRout, IRin

(ii) a. JE label
T_5 PCout, Yin, if (ZF=0) END
T_6 IRout, f1, Zin
T_7 Zout, PCin, END

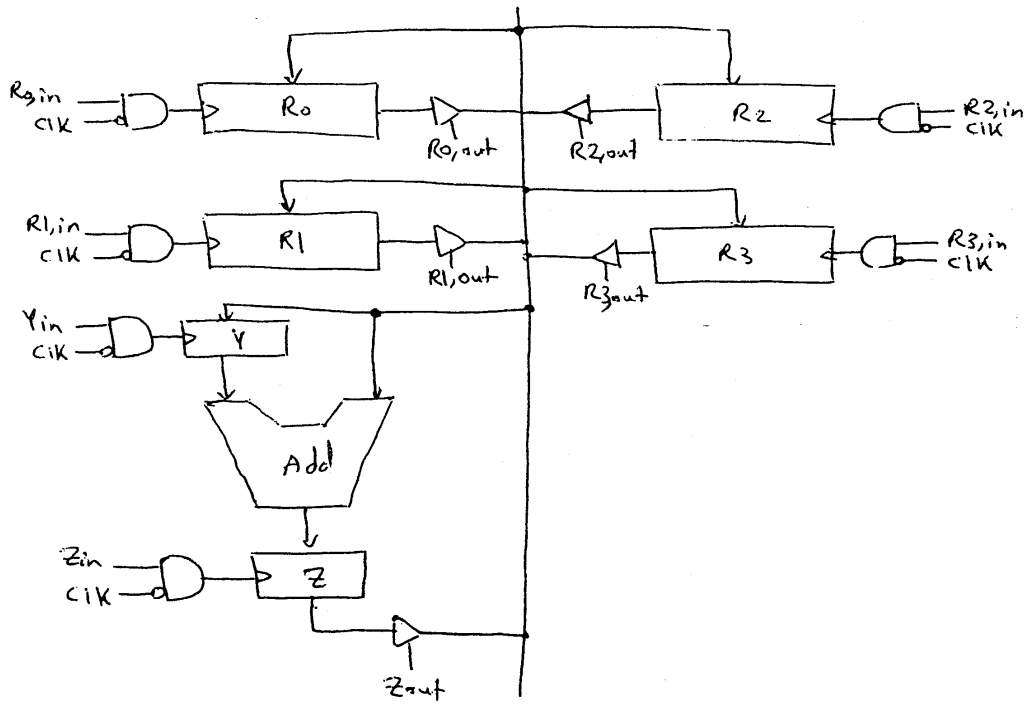
b. SUB J, 5
T_5 IRout, MARin, Read, WMFC
T_6 MDRout, Yin
T_7 IRout, f2, Zin
T_8 Zout, MDRin, write, WMFC
T_9 END

c. XCHG R1, R2
T_5 R1out, Tempin
T_6 R2out, R1in
T_7 Tempout, R2in, END

d. Loop label
T_5 R0,out, Yin
T_6 f4, Zin
T_7 Zout, R0in, if (ZF=1) end
T_8 PCout, Yin
T_9 IRout, f1, Zin
T_{10} Zout, PCin, end

(iii) $PCin = T_3 + JE \cdot T_7 + Loop \cdot T_{10}$

Q2. It is required to design a data path to execute the following two types of instructions: *MOV Rdst, Rsrc* and *ADD Rdst, Rsrc*, where *Rsrc* and *Rdst* can be either R0, R1, R2, or R3. Show the data-path design and indicate all the signals needed to control it. Note that you only need to show the interconnection of the registers with the adder i.e., there is no need to show the PC, IR, MAR and MDR registers.



Note that the signals R0,out, R1,out, R2,out, and R3,out are derived from the signals Rsrc,out, Rdst,out and the content of IR. Similarly, the signals R0,in, R1,in, R2,in, and R3,in are derived from the signal Rdst,in and the content of IR.