Name: **Id#**

COE 205, Term 101

Computer Organization & Assembly Programming

Quiz# 6

Date: Saturday, Jan. 1, 2011

Q1. Assume that a CPU has **16 instructions** with an opcode of 4 bits, seven **16-bit** general purpose registers namely AX, BX, CX, DX, SI, DI and SP, a **16-bit data bus**, and a **16-bit address bus**. Assume that all the instructions are 16-bit. The CPU has an **Arithmetic and Logic Unit (ALU)** with inputs A and B and output C, that can perform any of the following functions shown below based on the three selection lines AS2, AS1, and AS0:

AS2 AS1 AS0	Operation
000	C=A+B
001	C=A-B
010	C=A+1
011	C=A-1
100	C=B
101	C=A+2
110	C=A-2
111	C=NOT A

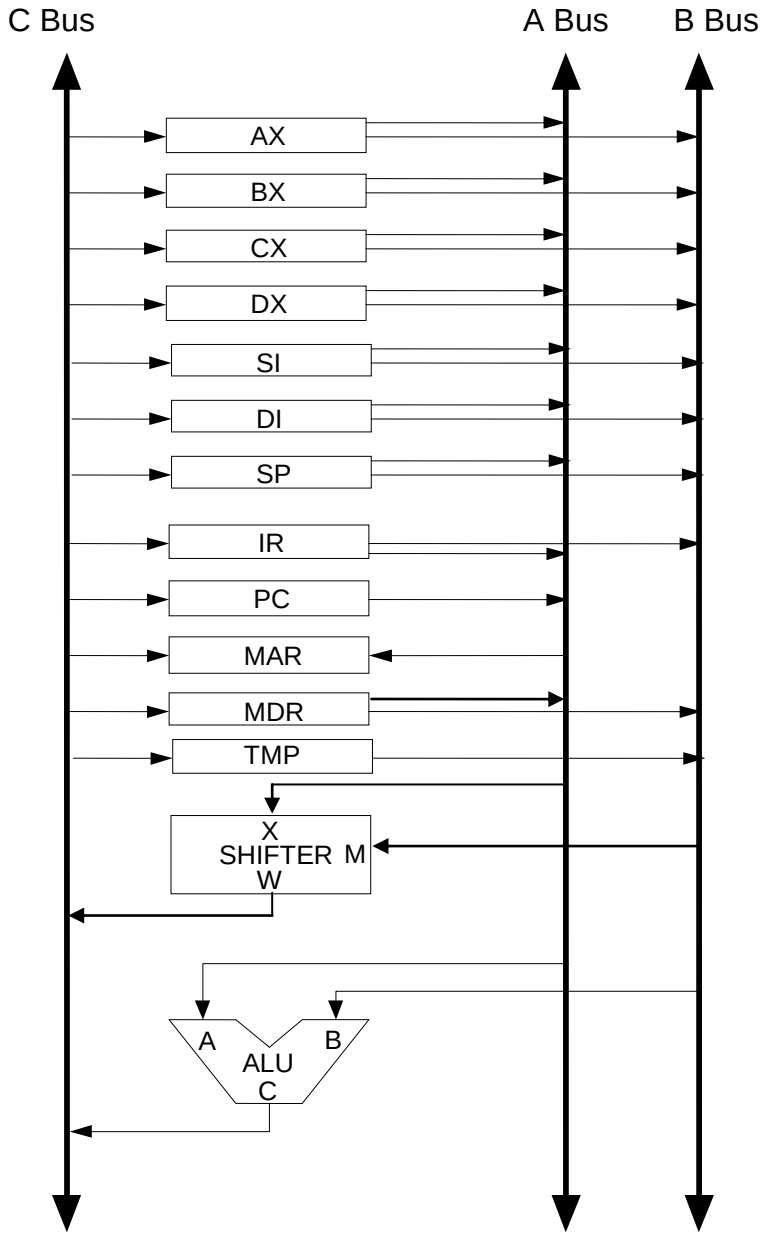
The CPU has also a **Shift Unit** that can perform shifting as shown below based on the two selection lines SS1 and SS0:

SS1 SS0	Operation
00	No shift
01	W=Shift logic right(X) by M bits
10	W=Shift logic left(X) by M bits
11	W=Shift arithmetic right(X) by M bits

Assume that the IR, PC, MAR, and MDR registers are also **16-bit regiters**. Also assume that the instructions for this processor follow the syntax and semantics and addressing modes of the 8086 processor. Also assume that registers play the same role as assumed in the 8086 processor.

Assume that the data path of this processor is implemented using a **three-bus architecture** as shown in the next page.

(i) Write the minimum number of control steps required for fetching an instruction from memory.



Data Path Design

(ii) Write the minimum number of control steps required for the execution of each of the following instructions:

a. **MOV AX, Array[BX]**

b. **ADD AX, 10**

c. **SUB [BX], AX**

d. **JE Next**

e. **SHL AX, 8**

f. **CALL NEXT**

g. **LOOPNE Next**