Name: **Id#**

COE 205, Term 993

Computer Organization & Assembly Programming
Quiz# 4

Date: Sunday, July 30

Q1. Consider the one-bus CPU organization shown below. Assume that the CPU has only three general registers, namely R0, R1, and R2. Furthermore, assume that the ALU can perform any of the following four functions based on the control signals *f1, f2, f3,* and *f4,* as shown below:

  f1: C=A+B;   *f2*: C=A-B;   *f3*: C=A+1;   *f4*: C=A-1;

(i)   Write the minimum number of control steps required to **fetch** an instruction using this CPU. Assume that the memory is asynchronous and that each instruction occupies one memory location.

(ii)   Write the minimum number of control steps required to **execute** each of the following instructions:

> (a) CMP R1, 20 ; compare the content of register R1 with the constant value 20.
>
> (b) ADD J, R2 ; add the content of memory variable J and the content of register R2 and store the result in J.
>
> (c) XCHG R1, I ; exchange the content of register R1 and memory variable I;
>
> (d) LOOP label ; decrement the content of R0 and then branch conditionally to *label* if the zero flag equals to 0. The branch address is specified using relative addressing mode.

(iii)   Assuming that the instruction set of the CPU consists of only the four instructions mentioned above, determine the logic needed in the encoder of a hardwired control unit for the signal *MAR$_{in}$*.

Q2. Consider the CPU-Memory interface circuit shown below. Complete the timing diagram of the read operation shown below.

CLK

Read

WMFC

MFC

MR

Run