Name: **Id#**

COE 205, Term 991

Computer Organization & Assembly Programming
Quiz# 4

Date: Wednesday, May. 10

Q1. Consider the one-bus CPU organization shown below. Assume that the CPU has only three general registers, namely R0, R1, and R2. Furthermore, assume that the ALU can perform any of the following four functions based on the control signals *f1*, *f2*, *f3*, and *f4*, as shown below:

f1: C=A+B; *f2*: C=A-B; *f3*: C=A+1; *f4*: C=A-1;

(i) Write the minimum number of control steps required to **fetch** an instruction using this CPU. Assume that the memory is asynchronous and that each instruction occupies one memory location.

(ii) Write the minimum number of control steps required to **execute** each of the following instructions:

(a) SUB R1, 20 ; subtract the constant value 20 from R1 and store the result in R1.

(b) INC J ; increment the content of memory variable J.

(c) MOV I, R1 ; move the content of register R1 to memory variable I;

(d) LOOP label ; decrement content of R0 and then branch conditionally to *label* if the zero flag equals to 0. The branch address is specified using relative addressing mode.

(iii) Assuming that the instruction set of the CPU consists of only the four instructions mentioned above, determine the logic needed in the encoder of a hardwired control unit for the signal MAR_{in}.

Q2. Consider the CPU-Memory interface circuit shown below. Complete the timing diagram of the read operation shown below.