Name: KEY **Id#**

COE 205, Term 092

Computer Organization & Assembly Programming

Quiz# 3

Date: Saturday, March 18, 2010

Q1. Fill the blank in each of the following:

1. The address bus of the 8086 processor is 20 bits while the data bus is 16 bits.

2. The address bus of the Pentium IV processor is 36 bits while the data bus is 64 bits.

3. A 3-way superscalar processor can execute 3 instructions per clock cycle.

4. The Pentium IV processor has 8 general purpose registers, 6 segment registers and EIP EFLAGS registers.

5. Characteristics of RISC processors include small and simple instruction set, all instructions have the same width and decoded and executed directly by hardware.

6. The address of the instruction to be fetched from memory is stored in the instruction pointer register (EIP).

7. Assuming that EIP=00000010, after fetching the instruction MOV AX, 1 (machine code: B80001) EIP= 00000010+3=00000013.

8. Assuming one clock cycle per pipeline stage, executing 1000 instructions in a 5 stage pipeline without any pipeline interruptions will take 5+999=1004 cycles.

9. Assuming real mode and that IP=0010,SI=0050, DI=3000, SP=2000 CS=00FF, DS=1010, SS=011F, the linear address of the next instruction to be fetched from memory is 00FF0+ 00010=01000.

10. Suppose that all segments from seg#0 until seg#200 are used. The segment number that will be allocated for an 8Kbyte code segment is 201 and for a 2Kbyte data segment is 401.

    Segment #201 starts at location 02010. A code segment of 8Kbytes requires offset in the range 00000 to 01FFF. Thus all the addresses from 00201 to (02010+01FFF=0400F). Thus, the next available address is 04010. Hence the data segment will be allocated segment#401.

11. In real mode, the logical address consists of segment number and offset address.

12. In protected mode, the linear address is computed based on adding a 32-bit offset with a 32-bit base address obtained from descriptor table indexed by segment selector.

13. A segment descriptor table stores for each segment 32-bit base address, 20-bit segment size and access rights.

14. Paging divides the linear address space into fixed-sized blocks called pages.

15. The operating system uses page tables to map the pages in the linear virtual address space onto main memory.