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COE 205, Term 082

Computer Organization & Assembly Programming

Quiz# 3

Date: Monday, April 6, 2009

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Q1. Determine three main differences between RISC and CISC processors and given an example processor of each type.

- ❖ CISC – Complex Instruction Set Computer
  - ✧ Large and complex instruction set
  - ✧ Variable width instructions
  - ✧ Requires microcode interpreter
    - ▪ Each instruction is decoded into a sequence of micro-operations
  - ✧ Example: Intel x86 family
- ❖ RISC – Reduced Instruction Set Computer
  - ✧ Small and simple instruction set
  - ✧ All instructions have the same width
  - ✧ Simpler instruction formats and addressing modes
  - ✧ Decoded and executed directly by hardware
  - ✧ Examples: ARM, MIPS, PowerPC, SPARC.

Q2. List the main general purpose and segment registers in the IA-32 processors.

Eight 32-bit general-purpose registers: EAX, EBX, ECX, EDX, ESI, EDI, EBP, ESP
Six 16-bit segment registers: CS, DS, SS, ES, FS, GS

Q3. Briefly explain the fetch-execute cycle.

In the fetch phase, the address of the instruction to be fetched is taken from the Instruction Pointer (IP) register and an instruction is read from memory and stored in an Instruction Register (IR). Then, the IP is incremented by the size of the fetched instruction.
In the execute phase, the instruction is decode and the control signals are generated, then the operands are fetched, the operation is executed and finally the result is stored back.

Q4. Given a processor with an 11-stage pipeline and clock frequency of 4 GHZ. Determine the time that will be required to execute a program of 1 billion instructions assuming that there will be no pipeline stalls.

The number of cycles required to execute the program is 10 + 1 billion ≈ 1 billion
Time of one clock cycle = 1/4 GHZ = 0.25 x 10^{-9} seconds.
Time for executing the program = 1 billion x 0.25 x 10^{-9} = 0.25 s.

Q5. Assume that a program has 4 Kbyte code and 5 Kbyte data. In Real Mode, assume that the first available free segment assigned for the code is segment#1005. Determine the segment that will be allocated to the data.

4 Kbyte = 1000h
The code segment spans the address space from 10050 to 10050+00fff=1104f
Thus, the first available segment allocated for data is segment 1105.

Q6. Explain logical to linear address translation in both real mode and protected mode.

In read mode, the segment registers determine the starting address of a segment = Segment ×
10 (hex). Linear address = Segment × 10 (hex) + Offset
In protected mode, the segment registers act as segment selectors. The upper 13 bits of a segment selector are used to index a descriptor table (GDT or LDT). This provides a 32-bit base address which is the starting address of a segment.
Then, linear address = base address + Offset.