Name: **Id#**

COE 205, Term 092

Computer Organization & Assembly Programming

Quiz# 3

Date: Saturday, March 18, 2010

Q1. Fill the blank in each of the following:

1. The address bus of the 8086 processor is _____ bits while the data bus is _____ bits.

2. The address bus of the Pentium IV processor is _____ bits while the data bus is _____ bits.

3. A 3-way superscalar processor can execute _____ instructions per clock cycle.

4. The Pentium IV processor has _____ general purpose registers, _____ segment registers and _____, _____ registers.

5. Characteristics of RISC processors include _____, _____ and _____.

6. The address of the instruction to be fetched from memory is stored in _____.

7. Assuming that EIP=00000010, after fetching the instruction MOV AX, 1 (machine code: B80001) EIP= _____.

8. Assuming one clock cycle per pipeline stage, executing 1000 instructions in a 5 stage pipeline without any pipeline interruptions will take _____ cycles.

9. Assuming real mode and that IP=0010,SI=0050, DI=3000, SP=2000 CS=00FF, DS=1010, SS=011F, the linear address of the next instruction to be fetched from memory is _____.

10. Suppose that all segments from seg#0 until seg#200 are used. The segment number that will be allocated for an 8Kbyte code segment is _____and for a 2Kbyte data segment is _____.

11. In real mode, the logical address consists of _____.

12. In protected mode, the linear address is computed based on adding _____ with _____ obtained from _____ indexed by _____.

13. A segment descriptor table stores for each segment _____, _____ and _____.

14. Paging divides the linear address space into _____.

15. The operating system uses _____ to map the pages in the linear virtual address space onto main memory.