Name: Id#

COE 205, Term 092

Computer Organization & Assembly Programming

Quiz# 3

 Date: Saturday, March 18, 2010

#

# **Q1.** Fill the blank in each of the following:

# The address bus of the 8086 processor is \_\_\_\_\_\_\_\_\_\_\_\_\_\_ bits while the data bus is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ bits.

#  The address bus of the Pentium IV processor is \_\_\_\_\_\_\_\_\_\_\_\_\_\_ bits while the data bus is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ bits.

# A 3-way superscalar processor can execute \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ instructions per clock cycle.

# The Pentium IV processor has \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ general purpose registers, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ segment registers and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ registers.

#  Characteristics of RISC processors include \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The address of the instruction to be fetched from memory is stored in \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Assuming that EIP=00000010, after fetching the instruction MOV AX, 1 (machine code: B80001) EIP= \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Assuming one clock cycle per pipeline stage, executing 1000 instructions in a 5 stage pipeline without any pipeline interruptions will take \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ cycles.

# Assuming real mode and that IP=0010,SI=0050, DI=3000, SP=2000 CS=00FF, DS=1010, SS=011F, the linear address of the next instruction to be fetched from memory is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Suppose that all segments from seg#0 until seg#200 are used. The segment number that will be allocated for an 8Kbyte code segment is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_and for a 2Kbyte data segment is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# In real mode, the logical address consists of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# In protected mode, the linear address is computed based on adding \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ with \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ obtained from \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ indexed by \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

#  A segment descriptor table stores for each segment \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

#  Paging divides the linear address space into \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The operating system uses \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ to map the pages in the linear virtual address space onto main memory.