Name: **Id#**

COE 205, Term 082

Computer Organization & Assembly Programming

Quiz# 3

Date: Monday, April 6, 2009

Q1. Determine three main differences between RISC and CISC processors and given an example processor of each type.

Q2. List the main general purpose and segment registers in the IA-32 processors.

Q3. Briefly explain the fetch-execute cycle.

Q4. Given a processor with an 11-stage pipeline and clock frequency of 4 GHZ. Determine the time that will be required to execute a program of 1 billion instructions assuming that there will be no pipeline stalls.

Q5. Assume that a program has 4 Kbyte code and 5 Kbyte data. In Real Mode, assume that the first available free segment assigned for the code is segment#1005. Determine the segment that will be allocated to the data.

Q6. Explain logical to linear address translation in both real mode and protected mode.