

Name: KEY

Id#

COE 205, Term 101
Computer Organization & Assembly Programming
Quiz#2

Date: Wednesday, Oct. 20, 2010

Q1. Fill the blank in each of the following:

1. The address bus of the Pentium IV processor is 36 bits while the data bus is 64 bits.
2. Characteristics of RISC processors include small and simple instruction set and all instructions have the same width.
3. Characteristics of CISC processors include large and complex instruction set and variable width instructions.
4. The Pentium IV processor has 8 32-bit general purpose registers, namely EAX, EBX, ECX, EDX, ESP, EBP, ESI, EDI.
5. The Instruction Pointer (EIP) register holds the address of the next instruction to be fetched from memory.
6. Each machine language instruction is first fetched from the memory and stored in an instruction register (IR).
7. Assuming that $EIP=0000101F$, after fetching a 5-byte instruction $EIP=$ $0000101F+5=00001024$.

8. Assuming one clock cycle per pipeline stage, executing 100 instructions in an 8-stage pipeline without any pipeline interruptions will take $8+99=107$ cycles.

9. Assuming real mode and that $IP=20E5$, $CS=03FC$, the linear address of the next instruction to be fetched from memory is $03FC0+20E5=060A5$.

10. Suppose that all segments from $seg\#0$ until $seg\#100$ are used. The segment number that will be allocated for a 3 Kbyte code segment is 101 and for a 1 Kbyte data segment is 1C1.

11. Segment unit translates logical address to linear address using segment descriptor table.

12. Paging unit translates linear address to physical address using a page directory and a page table