Name: KEY Id#

COE 205, Term 091

Computer Organization & Assembly Programming

Quiz# 2

 Date: Monday, Nov. 9, 2009

# **Q1.** Fill the blank in each of the following:

# The 8086 processor is a 16-bit machine with an address bus of 20 bits and a data bus with 16 bits.

# The Pentium 4 processor is a 32-bit machine with an address bus of 36 bits and a data bus with 64 bits.

# Reduced Instruction Set Computers (RISC) are based on having small and simple instruction set and have fixed width instructions.

#  Complex Instruction Set Computers (CISC) are based on having large and complex instruction set and have variable width instructions.

# The IA-32 has eight 32-bit general purpose registers, six 16-bit segment registers, Processor Status and Flags (EFLAGS) register and Instruction Pointer (EIP) register.

# Programmers can access the registers EAX, EBX, ECX and EDX either as 32-bit registers, or can access their 16-bit or 8-bit parts.

# The overflow flag is set when signed arithmetic result is out of range.

# The carry flag is set when unsigned arithmetic result is out of range.

# The sign flag is set when result is negative.

# The zero flag is set when result is zero.

# The parity flag is set when least-significant byte in result contains even number of 1s.

# The address of the instruction to be fetched is stored in a register called the Instruction Pointer (EIP).

# Given a 5-stage pipeline where each stage executes in one clock cycle, a clock cycle time of 1 ns (i.e. 10-9 sec), the time needed for executing 1 billion instructions without any pipeline stall is nearly 1 sec.

# Suppose that the memory addresses occupied so far is from 00000 to 020F1. The first available free segment is segment# 0210.

# Assume that DS=12FF, CS=E6F0, ES=F135, SS=ABCD, IP=0016, and SI=526F. The physical address of the next instruction to be fetched from memory in real address mode is E6F00+00016=E6F16.

# In real address mode, the starting physical address for segment number 20h is 00200 and the ending physical address is 00200+0FFFF=101FF.

# In protected mode, the logical address consists of 16-bit segment selector and 32-bit offset.

#  In protected mode, the segment unit translates logical address to linear address using a segment descriptor table and the paging unit translates linear address to physical address.