Name: KEY **Id#**

COE 205, Term 071

Computer Organization & Assembly Programming

Quiz# 2

Date: Saturday, Oct. 27, 2007

Q1. Fill the blank in each of the following questions:

1. The size of the **address bus** in the **8086** processor is **20** bits while in the **Pentium IV** Processor it is **36** bits.

2. The size of the **data bus** in the **8086** processor is **16** bits while in the **Pentium IV** Processor it is **64** bits.

3. The IA-32 registers consist of **8** 32-bit general-purpose registers, **6** 16-bit segment registers, the **EIP** register and the **status & flags** register.

4. Adding the following two 16-bit numbers F0F8+EF8A has the following values on the flags: CF=**1**, ZF=**0**, SF=**1**, AF=**1**, PF=**1**, OF=**0**. **(Result=E082)**

5. The address of the instruction to be fetched is stored in a register called **Instruction Pointer.**

6. After reading an instruction whose size is **64 bits**, the **instruction pointer** is incremented by **8**.

7. Each machine language instruction is first fetched from memory and stored in the **Instruction Register**.

8. A processor is considered **superscalar** when **it can execute more than one instruction per clock cycle.**

9. RISC processors have the following characteristics: **small and simple instruction set, all instructions have the same width, simpler instruction formats and addressing modes, instructions decoded and executed directly by hardwar**e

10. 16-bit and 8-bit parts of the registers **EAX, EBX, ECX, EDX** can be accessed by programmers.

11. With a 5-stage pipeline with each stage requiring one clock cycle for execution, the number of clock cycles needed to execute 10 instructions is **5+10-1=14**.

12. In real address mode, the staring address of segment#10CD is **10CD0** and the maximum ending address is **10CD0+0FFFF=20CCF**.

13. In real address mode with a logical address given as 10A2:30A0, the linear address is **=10A20+030A0=13AC0.**

14. In Flat Memory model, all segments are mapped to **the same linear** address space.

15. In protected mode, linear address is translated to physical address using **paging.**

16. **Assembler directives** provide information to the assembler while translating a program.

Q2. Suppose that the following data declarations are allocated in the data segment.

```
I       BYTE        32, '32'
J       WORD        1234H, -10
K       EQU         1
ALIGN 4
L       DWORD       K-5
M       BYTE        2  dup(2, 2 dup(1))
```

(i) Show the content of the allocated memory, in hexadecimal. Note that the ASCII code of character 'A' is 41H and that of 'a' is 61H. Also, the ASCII code of character '0' is 30H.

Variable	*Memory Address (Hex)*	*Memory Content (Hex)*
I	*00404000*	*20*
	00404001	*33*
	00404002	*32*
J	*00404003*	*34*
	00404004	*12*
	00404005	*F6*
	00404006	*FF*
	00404007	*Skipped due to alignment*
L	*00404008*	*FC*
	00404009	*FF*
	0040400A	*FF*
	0040400B	*FF*
M	*0040400C*	*02*
	0040400D	*01*
	0040400E	*01*
	0040400F	*02*
	00404010	*01*
	00404011	*01*
	00404012	

(ii) Determine the content of **destination** registers after executing each of the given instructions:

1. MOV AL, I+1 **AL=33**

2. MOV EBX, OFFSET J **EBX=00404003**

3. MOV CH, TYPE L **CH=4**

4. MOV EDX, SIZEOF J **EDX=4**

5. MOV EDX, LENGTHOF J **EDX=2**

6. MOV DH, BYTE PTR J+1 **DH=12**