Name: **Id#**

COE 205, Term 101

Computer Organization & Assembly Programming

Quiz#2

Date: Wednesday, Oct. 20, 2010

Q1. Fill the blank in each of the following:

1. The address bus of the Pentium IV processor is _____ bits while the data bus is _____ bits.

2. Characteristics of _____ processors include small and simple instruction set and all instructions have the same width.

3. Characteristics of _____ processors include large and complex instruction set and variable width instructions.

4. The Pentium IV processor has 8 32-bit general purpose registers, namely _____ _____.

5. The Instruction Pointer (EIP) register holds _____.

6. Each machine language instruction is first fetched from the memory and stored in an _____.

7. Assuming that EIP=0000101F, after fetching a 5-byte instruction EIP= _____.

8. Assuming one clock cycle per pipeline stage, executing 100 instructions in an 8-stage pipeline without any pipeline interruptions will take _____ cycles.

9. Assuming real mode and that IP=20E5, CS=03FC, the linear address of the next instruction to be fetched from memory is _____.

10. Suppose that all segments from seg#0 until seg#100 are used. The segment number that will be allocated for a 3 Kbyte code segment is _____and for a 1 Kbyte data segment is _____.

11. Segment unit translates _____ to _____ using _____.

12. Paging unit translates_____ to _____ using a page directory and a page table