Name: Id#

COE 205, Term 101

Computer Organization & Assembly Programming

Quiz#2

 Date: Wednesday, Oct. 20, 2010

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# **Q1.** Fill the blank in each of the following:

#  The address bus of the Pentium IV processor is \_\_\_\_\_\_\_\_\_\_\_\_\_\_ bits while the data bus is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ bits.

# Characteristics of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ processors include small and simple instruction set and all instructions have the same width.

# Characteristics of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ processors include large and complex instruction set and variable width instructions.

# The Pentium IV processor has 8 32-bit general purpose registers, namely \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The Instruction Pointer (EIP) register holds \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Each machine language instruction is first fetched from the memory and stored in an **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**.

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# Assuming that EIP=0000101F, after fetching a 5-byte instruction EIP= \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Assuming one clock cycle per pipeline stage, executing 100 instructions in an 8-stage pipeline without any pipeline interruptions will take \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ cycles.

# Assuming real mode and that IP=20E5, CS=03FC, the linear address of the next instruction to be fetched from memory is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Suppose that all segments from seg#0 until seg#100 are used. The segment number that will be allocated for a 3 Kbyte code segment is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_and for a 1 Kbyte data segment is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

#  Segment unit translates \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ to \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ using \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

#  Paging unit translates\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ to \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ using a page directory and a page table