Name: Id#

COE 205, Term 091

Computer Organization & Assembly Programming

Quiz# 2

 Date: Monday, Nov. 9, 2009

# **Q1.** Fill the blank in each of the following:

# The 8086 processor is a \_\_\_\_\_\_\_\_\_\_\_\_\_ bit machine with an address bus of \_\_\_\_\_\_\_\_ bits and a data bus with \_\_\_\_\_\_\_\_\_\_\_\_ bits.

# The Pentium 4 processor is a \_\_\_\_\_\_\_\_\_\_\_\_\_ bit machine with an address bus of \_\_\_\_\_\_\_\_ bits and a data bus with \_\_\_\_\_\_\_\_\_\_\_\_ bits.

# \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ are based on having small and simple instruction set and have fixed width instructions.

#  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ are based on having large and complex instruction set and have variable width instructions.

# The IA-32 has \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ general purpose registers, \_\_\_\_\_\_\_\_\_\_\_\_ segment registers, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Programmers can access the registers \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ either as 32-bit registers, or can access their 16-bit and 8-bit parts.

# The overflow flag is set when \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The carry flag is set when \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The sign flag is set when \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The zero flag is set when \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The parity flag is set when \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# The address of the instruction to be fetched is stored in a register called \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Given a 5-stage pipeline where each stage executes in one clock cycle, a clock cycle time of 1 ns (i.e. 10-9 sec), the time needed for executing 1 billion instructions without any pipeline stall is nearly \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ sec.

# Suppose that the memory addresses occupied so far is from 00000 to 020F1. The first available free segment is segment#\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# Assume that DS=12FF, CS=E6F0, ES=F135, SS=ABCD, IP=0016, and SI=526F. The physical address of the next instruction to be fetched from memory in real address mode is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# In real address mode, the starting physical address for segment number 20h is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_and the ending physical address is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

# In protected mode, the logical address consists of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

#  In protected mode, the segment unit translates logical address to linear address using \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and the \_\_\_\_\_\_\_\_\_\_\_unit translates linear address to physical address.