Name: **Id#**

COE 205, Term 071

Computer Organization & Assembly Programming

Quiz# 2

Date: Saturday, Oct. 27, 2007

Q1. Fill the blank in each of the following questions:

1. The size of the **address bus** in the **8086** processor is _____ bits while in the **Pentium IV** Processor it is _____ bits.

2. The size of the **data bus** in the **8086** processor is _____ bits while in the **Pentium IV** Processor it is _____ bits.

3. The IA-32 registers consist of _____ 32-bit general-purpose registers, _____ 16-bit segment registers, the _____ register and the _____register.

4. Adding the following two 16-bit numbers F0F8+EF8A has the following values on the flags: CF=_____, ZF=_____, SF=_____, AF=_____, PF=_____, OF=_____.

5. The address of the instruction to be fetched is stored in a register called **_____.**

6. After reading an instruction whose size is **64 bits**, the **instruction pointer** is incremented by _____.

7. Each machine language instruction is first fetched from memory and stored in _____.

8. A processor is considered **superscalar** when **_____.**

9. RISC processors have the following characteristics: _____, _____, _____, _____

10. 16-bit and 8-bit parts of the registers _____, _____, _____, _____ can be accessed by programmers.

11. With a 5-stage pipeline with each stage requiring one clock cycle for execution, the number of clock cycles needed to execute 10 instructions is _____.

12. In real address mode, the staring address of segment#10CD is _____ and the maximum ending address is _____.

13. In real address mode with a logical address given as 10A2:30A0, the linear address is _____.

14. In Flat Memory model, all segments are mapped to _____ address space.

15. In protected mode, linear address is translated to physical address using _____.

16. _____ provide information to the assembler while translating a program.

Q2. Suppose that the following data declarations are allocated in the data segment.

```
I       BYTE        32, '32'
J       WORD        1234H, -10
K       EQU          1
ALIGN 4
L       DWORD       K-5
M       BYTE        2  dup(2, 2 dup(1))
```

(i) Show the content of the allocated memory, in hexadecimal. Note that the ASCII code of character 'A' is 41H and that of 'a' is 61H. Also, the ASCII code of character '0' is 30H.

Variable	*Memory Address (Hex)*	*Memory Content (Hex)*
	00404000	
	00404001	
	00404002	
	00404003	
	00404004	
	00404005	
	00404006	
	00404007	
	00404008	
	00404009	
	0040400A	
	0040400B	
	0040400C	
	0040400D	
	0040400E	
	0040400F	
	00404010	
	00404011	
	00404012	

(ii) Determine the content of **destination** registers after executing each of the given instructions:

1. MOV AL, I+1

2. MOV EBX, OFFSET J

3. MOV CH, TYPE L

4. MOV EDX, SIZEOF J

5. MOV EDX, LENGTHOF J

6. MOV DH, BYTE PTR J+1