Name: KEY **Id#**

COE 205, Term 043

Computer Organization & Assembly Programming

Quiz# 1

Date: Saturday, July 9, 2005

Q1. Explain the function of each of the following:

i. Instruction Pointer (IP).

A register that holds that address of the next instruction to be fetched from memory.

ii. Instruction Register (IR).

A register that holds that instruction fetched from memory.

iii. Assembler.

A program that translates assembly language to machine language.

iv. Memory Address Register (MAR).

A register connected to the address bus and holds the address of memory location that is to be read from or written to.

Q2. Describe what is meant by the Instruction Set Architecture (ISA) of a computer.

The Instruction Set Architecture of a computer is the set of instructions of the computer, the memory and the programmer accessible registers.

Q3. Which of the following 8086 registers is part of the ISA: **Instruction Pointer (IP), Instruction Register (IR), Memory Data Register (MDR), CX, SI, Y**.

IP, CX, SI

Q4. Determine the machine type and the size of the address bus and the data bus for the **8086** and the **Pentium IV** processors.

Processor	Machine Type	Address Bus	Data Bus
8086	16-bit	20-bit	16-bit
Pentium IV	32-bit	36-bit	64-bit

Q5. Determine whether the following operations are performed in the fetch or execute phase: **Reading an instruction from Memory, Reading and Writing Operands from/to Memory, Incrementing the Program Counter, Performing Arithmetic Operations e.g. subtraction.**

Operation	Phase
Reading an instruction from Memory	Fetch
Reading and Writing Operands from/to Memory	Execute
Incrementing the Program Counter	Fetch
Performing Arithmetic Operations e.g. subtraction	Execute

Q6. Order the following storage devices once in terms of **speed** and once in terms of **capacity**: RAM, Registers, Hard Disk, and Cache.

SPEED: Registers, Cache, RAM Hard Disk (order from highest speed to lower)

CAPACITY: Hard Disk, RAM, Cache, Registers (order from higher capacity to lower)