Name: **Id#**

COE 205, Term 051

Computer Organization & Assembly Programming

Quiz# 1

Date: Monday, Sep. 26, 2005

Q1. Fill the blank in each of the following questions:

1. The _____ register holds the address of the next instruction to be fetched from memory.
2. The _____ register holds the fetched instruction to be executed.
3. The _____ register is connected to the **address bus** in the CPU memory interface.
4. The _____ register is connected to the **data bus** in the CPU memory interface.
5. The **Instruction Set Architecture** (ISA) of a computer consists of _____, _____, and _____.
6. The size of the **address bus** in the **8086** processor is _____ bits while in the **Pentium** Processor it is _____ bits.
7. The size of the **data bus** in the **8086** processor is _____ bits while in the **Pentium** Processor it is _____ bits.
8. **Reading an instruction** from Memory is performed in the _____ phase.
9. **Reading operands** from Memory is performed in the _____ phase.
10. **Incrementing the Instruction Pointer** is performed in the _____ phase.

11. **Decoding an instruction** is performed in the _____ phase.

12. With an **address bus size** equal to **32 bits**, the memory address space is _____ Bytes.

13. With a **data bus size** equal to **32 bits**, the maximum number of bytes that is transferred between the CPU and memory per a read/write cycle is _____ Bytes.

14. After reading an instruction whose size is **16 bits**, the **instruction pointer** is incremented by _____.

15. The CPU is divided into two main units called _____ and _____.

16. Two of the reasons for why it is important to program in Assembly Language are _____
_____
and
_____
_____.

17. The **Cache memory** is faster than _____ and slower than _____.

18. The program that translates assembly language into machine language is called _____.