COE 205, Term 992

Computer Organization & Assembly Programming

HW# 6

Due date: Saturday, May 6

Q.1. Show the memory cell array and required logic for the structure of a 4x1 bit RAM designed as:

(a) One-dimensional array.

(b) Two-dimensional array.

Q.2. Write the sequence of control steps required for the one-bus organization discussed in class for each of the following instructions. Write the fetch phase only once, then write the execute phase for each instruction.
Assume that each instruction occupies two memory locations while each data occupies only one memory location. Also, assume that the memory access is asynchronous.

(a) ADD R1, 10 ; add immediate to R1.

(b) ADD R1, var1 ; add content of the memory location var1 to R1.

(c) ADD [var1], R1 ; add R1 to content of memory using indirect addressing mode.

(d) JNZ label1 ; jump to label1 if zero flag is 0, where value of label1 is determined by adding a displacement with the instruction to IP.

Q.3. Repeat **Q.2 (c)** assuming that the memory access is synchronous and that the read/write memory operation takes two internal CPU cycles. Write only the execute phase.

Q.4. Write the sequence of control steps required for the two-bus and three-bus organizations discussed in class for the instruction in **Q.2 (a)**, respectively. Then, compute the speedup gained for this instruction in each case, compared to the one-bus organization. Assume that the propagation time across tri-state buffers is 5ns, bus propagation time is 5ns, ALU propagation time is 14 ns, and flip-flop propagation time is 6ns.

Q.5. Assume that the instruction set of the single-bus CPU consists of only the four instructions mentioned in **Q.2**.

(a) Determine the logic needed in the encoder of a hardwired control unit for the ALU signal ADD and for the signal END.

(b) Show the control word needed for the CPU assuming a microprogrammed control unit.