March 27, 2010

COMPUTER ENGINEERING DEPARTMENT

COE 205

COMPUTER ORGANIZATION & ASSEMBLY PROGRAMMING

Major Exam I

Second Semester (092)

Time: 8:00-10:00 PM

Student Name : ____

Student ID. : ____

Question	Max Points	Score
Q1	76	
Q2	12	
Q3	12	
Total	100	

Dr. Aiman El-Maleh

[76 Points]

(Q1) Fill the blank in each of the following:

(1) The advantages and disadvantages of programming in assembly language are ____.

(2) The advantages and disadvantages of DRAM are ____.

(3) The instruction set architecture of a processor is composed of ____.

(4) In protected mode, the logical address consists of ____.

(5) In protected mode, the linear address is computed based on ____.

(6) Given that variables I and J are Dword variables, their content can be swapped using the following instructions:

____

(7) Given that variable I is defined as Qword, the content of I is incremented using the following code:

____

(8) Given a magnetic disk with the following properties: Rotation Speed = 5000 RPM (rotations per minute), Average Seek = 4 ms, Sector = 512 bytes, Track = 250 sectors. The average time to access a block of 50 consecutive sectors is ____
____
____
____.

(9) The integer number -2000 is represented in hexadecimal using 16-bit 2's complement representation as ______________.

(10) Assuming 16-bit 2's complement representation, the hexadecimal number EC10 represents the decimal number____________________________________.

(11) Assuming 4-bit 2's complement representation, the largest number that can be stored is ________ in decimal and ________ in binary and the smallest number that can be stored is ________ in decimal and ________in binary.

(12) Given that the number 88h is represented using 8-bit 2's complement representation, the equivalent number represented using 16-bit 2's complement representation is ___________.

(13) Given that register AL=C4 stores an ASCII character, then the stored character is ________ and the used parity is _______. Note that 'A'=41h and 'a'=61h.

(14) The ____________ register holds the address of the next instruction to be fetched from memory.

(15) Given that the instruction ADD AX, I (having the machine code 03060000) is stored at address 0000002C, then the address of the next instruction to be fetched from memory is _________________.

(16) Given a processor with an 8-stage pipeline and clock frequency of 2 GHZ, the time that will be required to execute a program of 4 billion instructions assuming that there will be no pipeline stalls is nearly ____ seconds.

(17) Assume that the range of addresses from 00000 to 00A1A is used by another program. Given that a program has a code segment of 8 Kbyte and a data segment of 3 Kbyte, the code segment number allocated is ______________________ and the data segment number allocated is __________________________________.

(18) Assume that DS=00EF, CS=013A, ES=0112, SS=0FEC, IP=00FF, BX=309A, and SP=01FC. Based on 16-bit real-mode addressing, the linear address of the next instruction to be fetched from memory is ____.

(19) Assume that DS=00EF, CS=013A, ES=0112, SS=0FEC, IP=00FF, BX=309A, and SP=01FC. Based on 16-bit real addressing mode, the linear address of the source operand in the instruction MOV AX, [BX+5] is ____.

(20) The addressing mode of the source operand in the instruction MOV EAX, [MSG+1] is ______________________________.

(21) Assume that AX=00FFh. Executing the instruction INC AL produces the result AX=________________________.

(22) The addressing mode of the source operand in the instruction MOV SI, [EBX] is _________________________________.

(23) The assembler allocates ________ bytes for the variable *Array* defined below:

Array Dword 5 dup(30, 30 dup(0))

(24) The content of register EAX after executing the following instructions is_____________________.

```
I=5
J EQU 10
MOV EAX, I-J
I=I-3
ADD EAX, I+J
```

(25) Assuming the following data segment and assuming that variable X is given the linear address 00404000h, then the linear address for variables Y and Z will be ________________ and ________________.

```
.DATA
X       BYTE 1, 2, 3, 4, 5
ALIGN 4
Y       DWORD 4, 5
ALIGN  2
Z       WORD  7,  8, 9
```

(26) Assuming the following data segment and assuming that variable X is given the linear address 00404000h, then the content of register EAX after executing the instruction MOV EAX, Y-5 is _______________.

```
.DATA
X       BYTE "EXAM I", 0
        WORD 10, 20
Y       DWORD  30, 40
```

(27) Assuming the following data segment and assuming that variable X is given the linear address 00404000h , after executing the code given below, the content of register EAX=___________ and EBX=______________.

```
.DATA
X       WORD  10, 20, 30
Y       DWORD 30, 40, 50
.CODE
MOV EAX, TYPE Y
MOV EBX, OFFSET Y-2
```

(28) After executing the code given below, the content of registers EAX and EBX will be ______________ and _____________.

```
.DATA
ARRAY           DWORD           10, 20, 30,
                                40, 50, 60
.CODE
MOV EAX, LENGTHOF ARRAY
MOV EBX, SIZEOF ARRAY
```

(29) After executing the code given below, the content of register EAX will be ______________.

```
.DATA
ARRAY WORD  10, 20, 30, 40, 50, 60
.CODE
MOV EAX, DWORD PTR ARRAY+3
```

(30) Assuming that variable ARRAY is defined as shown below:

ARRAY DWORD 1, 2, 3, 4, 5, 6

The content of register AX after executing the instruction MOV EAX, ARRAY+2 will be ____________.

(31) Assume that AL=93h. Executing the instruction MOVSX EBX, AL produces the result EBX=________________.

(32) Assume that AX=A100h. Executing the instruction *NEG AX* produces the following results: AX=______, overflow flag=___, sign flag=___, zero flag=___, carry flag=___, auxiliary flag=___ and parity flag=___.

(33) Assume that AX=ABCDh and BX=8876h. Executing the instruction *ADD AX, BX* produces the following results: AX=______, overflow flag=___, sign flag=___, zero flag=___, carry flag=___, auxiliary flag=___ and parity flag=___.

(34) Assume that AX= 98A0h and BX= FFDAh. Executing the instruction *SUB AX, BX* produces the following results: AX=______, overflow flag=___, sign flag=___, zero flag=___, carry flag=___, auxiliary flag=___ and parity flag=___.

(35) The content of register EAX after executing the instructions below will be ___________________.

```
.DATA
    ARRAY           DWORD  1, 2, 3, 4
                    DWORD  5, 6, 7 , 8
                    DWORD  9, 10, 11, 12
    RS EQU   SIZEOF ARRAY
.CODE
    MOV ESI, 2*RS
    MOV EDI, 3
    MOV EAX, ARRAY[ESI+EDI*TYPE ARRAY]
```

[12 Points]

(Q2) Consider a program that has the following data segment assuming a flat memory model:

X	*EQU*	*16*
Y	*BYTE*	*17*
Z	*WORD*	*18*
W	*DWORD*	*19*

Indicate whether the following are valid **IA-32** instructions or not. **If invalid, give the reason**:

1. MOV EAX, W-1

2. MOV Z, Word PTR Y

3. MOV DS, X

4. MOV Z, X

5. MOV AX, OFFSET Z

6. MOVSX EAX, X

7. MOV W, Dword PTR AX

8. INC [EBX]

[12 Points]

(Q3) Suppose that the following directives are declared in the data segment with a starting linear address of 00404000. Show the linear addresses of allocated memory and their corresponding content in hexadecimal. Note that the ASCII code for character 'a' is 61h and that of character 'A' is 41h. The ASCII code of character '0' is 30h.

```
I    BYTE    10,"10",0
     WORD    10, -10
J    DWORD   112, -112
K    EQU     100
L    BYTE    K+20
     BYTE    2, 2 dup(1,-1)
```

Variable	Linear Address (Hex.)	Content (Hex.)
I	00404000	