KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 992 Lectures

	Date	Topics	Ref.	Lab
1	M 17/1	Syllabus. Introduction.	Handout	
2	W 19/1	The general purpose machine, Views of the computer: the user`s view, the machine/assembly language programmer`s view, the computer architect`s view. Instruction Set Architecture.	Handout	
3	S 22/1	***Computer structure***: CPU organization, memory organization, and I/O. ***Info. Representation***: Binary, Octal, Hex., 2`s complement representation.	2.2, Handout App. B	
	M 24/1			Introduction, using MASM
4	M 24/1	***Info. Representation***: 2`s complement addition/subtraction, range.	App. B	
5	W 26/1	***Assembly Concepts***: Overflow, ASCII characters, assembly directives and instructions. **(HW#1 Distributed**)	2.1, 2.3	
6	TH 27/1	***Assembly Concepts***: declaring variables (DB, DW, DD), constants (EQU), and arrays (DUP), type and size of information. 8086 memory.	2.3, 2.5, handout	
7	S 29/1	***Assembly Concepts:*** Assembly instruction format. I/O using DOS functions. INT 21H with functions 1, 2, 8, 9, and A. OFFSET operator.	3.3	
	M 31/1			I/O
8	M 31/1	***8086 registers and memory segmentation:*** list of 8086 registers and their use. Code, data, and stack segments. Offset address and physical address. LEA inst. **(HW#1 Collected**)	3.1, 3.2 handout	
9	W 2/2	***8086*** Flags (Carry, Zero, Sign, Overflow, Parity, Auxiliary). ***Assembly Concepts:*** Addressing modes. **(Quiz#1)**	3.1, 4.3, handout	
10	S 5/2	***Assembly Concepts:*** Addressing modes.	4.3, handout	
	M 7/2			Segmentation & addressing modes
11	M 7/2	Instruction types, MOV instruction. Data type, accessing memory. **(HW#2 Distributed**)	3.2, handout	

12	W 9/2	***8086 instructions***: MOV with indexing, XCHG, ADD, SUB.	3.2, handout	
13	S 12/2	***8086 instructions***: ADC, SBB, INC, DEC, NEG, CMP, CBW, CWD	3.2, handout	
	M 14/2			Indexing, data manipulation
14	M 14/2	***8086 instructions:*** MUL, IMUL **(HW#2 Collected**)	3.2, handout	
15	W 16/2	***8086 instructions:*** DIV, IDIV **(Quiz#2) (HW#3 Distributed**)	3.2, handout	
16	S 19/2	***8086 instructions:*** Logical instructions, AND, OR, XOR, NOT, TEST.	4.1, handout	
	M 21/2			Arithmetic, logical
17	M 21/2	***8086 instructions:*** Shift instructions, SHR, SAR, SHL/SAL.	4.1, handout	
18	W 23/2	***8086 instructions***: Rotate instructions, ROR, ROL, RCL, RCR. **(HW#3 Collected**)	4.1, handout	
19	S 26/2	***8086 instructions***: Compare CMP. Conditional jumps, JZ, JNZ, JE, JNE, JS, JNS, JO, JNO, JP, JNP.	3.5, handout	
	M 28/2			Shift, rotate, jump, loop
20	M 28/2	***8086 instructions:*** Conditional junps: signed and unsigned instructions. LOOP, LOOPE, LOOPNE . **(Exam I)**	3.5, handout	
21	W 1/3	***8086 instructions:*** Stack operations: PUSH, POP.	2.4, handout	
22	S 4/3	***8086 instructions:*** Subprograms and Macros. The execution of CALL, RET.	3.4, 4.2, 4.4 handout	
	M 6/3			Subroutines & macros
23	M 6/3	***8086 instructions:*** Parameter passing in subroutines. **(HW#4 Distributed**)	Handout	
24	W 8/3	***8086 instructions:*** String instructions, CLD, STD, MOVS.	Handout	
25	S 25/3	***8086 instructions:*** SCAS, CMPS, LODS, STOS, SCAS String instructions prefixes: REP, REPE, REPNE.	Handout	
	M 27/3			String instructions
26	M 27/3	I/O instructions, IN, OUT. ***Interrupts:*** hardware and software interrupts, INT instruction, interrupt type, interrupt vector table.	Handout	
27	W 29/3	***Interrupts:*** 8086 interrupt processing. **(HW#4 Collected**)	Handout	

28	S 1/4	***Computer Structure***: Bus system, data bus, address bus, control bus (command, timing, arbitration). **(Quiz#3)**	5.1, handout	
	M 3/4			Video memory
29	M 3/4	***Computer Structure***: memory hierarchy, random access, access time vs. cycle time, DRAM, SRAM.	5.1, handout	
30	W 5/4	***Computer Structure***: external memory, disks, direct access, average access time and transfer rate. Tapes, sequential access. CD-ROM **(HW#5 Distributed**)	5.1, handout	
31	S 8/4	Processor Design, register transfer, fetch-execute cycle.		
	M 10/4			Interrupts
32	M 10/4	Single-bus CPU. Register transfer timing.	Handout	
33	W 12/4	***Review for ExamII.*** **(HW#5 Collected**)		
34	S 15/4	***Memory-CPU interface:*** Synchronous vs. Asynchronous.	Handout	
	M 17/4			Using the mouse
35	M 17/4	Execution of add instruction, execution of unconditional and conditional branch instructions.	Handout	
36	W 19/4	***Performance considerations:*** 2-bus CPU & 3-bus CPU.	Handout	
37	S 22/4	***Control unit design:*** hardwired control unit organization, generation of control signals.	Handout	
	M 24/4			Project
38	M 24/4	CPU-Memory interaction circuit design, practical aspects of circuit implementation.	Handout	
39	W 26/4	Microprogrammed control: microprogrammed control unit operation, microroutines for add & branch on negative.	Handout	
40	S 29/4	Microprogramed control unit with conditional branching, Microinstruction format:field-encode. **(HW#6 Distributed**)	Handout	
	M 1/5			Project
41	M 1/5	Horizontal vs. Vertical control store, Nanocoding, Microcode branching example.	Handout	
42	W 3/5	***Microprogram Example***: Add instruction with addressing modes.	Handout	
43	S 6/5	Microinstruction sharing, multiway branching, wide branch addressing, Bit Oring. **(HW#6 Collected**)	Handout	
44	M 8/5	Microinstruction sequencing, Microinstruction format:Example, Control signal generation. Improving performance of microprogrammed control unit. **(Quiz#4)**	Handout	
45	W 10/5	Final Exam Review		