KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 991 Lectures

	Date	Topics	Ref.	Lab
1	M 6/09	Syllabus. Introduction.	notes	
2	W 8/09	***Computer structure***: CPU organization, memory organization, and I/O. ***Info. Representation***: Binary, Hex.	2.2, notes App. B	
3	S 11/09	***Info. Representation***: Octal. 2`s complement representation, range, addition.	App. B	
	M 13/09			introduction
4	M 13/09	***Info. Representation***: 2`s complement subtraction, overflow. ASCII characters. Introduction to computer software.	App. B, notes	
5	W 15/09	***Assembly Concepts***: Introduction to software. High level language vs. assembly and machine languages. Assembly directives and instructions. **(HW#1 Distributed**)	2.1, 2.3	
6	T 16/09	***Assembly Concepts***: declaring variables (DB, DW, DD), constants (EQU), and arrays (DUP), type and size of information. 8086 memory.	2.3, 2.5	
7	S 18/09	***Assembly Concepts:*** Assembly instruction format. I/O using DOS functions. INT 21H with functions 1, 2, and 9. OFFSET operator.	3.3	
	M 20/09			I/O
8	M 20/09	***Assembly Concepts:*** Addressing modes. **(HW#1 Collected**)	4.3, notes	
9	W 22/09	***Assembly Concepts:*** Addressing modes. **(Quiz#1)**	4.3, notes	
10	S 25/09	***8086 registers and memory segmentation:*** list of 8086 registers and their use. Offset address and physical address. **(HW#2 Distributed**)	3.1, notes	
	M 27/09			segmentation
11	M 27/09	***8086 memory segmentation:*** Code, data, and stack segments. Calculation of physical address.	3.2, notes	
12	W 29/09	***8086 instructions***: MOV instruction. Data type, accessing memory.	3.2, notes	
13	S 2/10	***8086 instructions***: MOV with indexing. ADD, SUB. **(HW#2 Collected**)	3.1, 3.2, notes	
	M 4/10			indexing,

				mov, add, sub
14	M 4/10	***8086 instructions***: Flags (Carry, Zero, Sign, Overflow, Parity, Auxiliary). ADC, SBB, INC, DEC. **(Quiz#2)**	3.2, notes	
15	W 6/10	***8086 instructions:*** examples on the use of ADC. MUL, IMUL. **(HW#3 Distributed**)	3.2, notes	
16	S 9/10	***8086 instructions:*** DIV, IDIV. Logical instructions, AND, OR, XOR, NOT, TEST.	3.2, 4.1, notes	
	M 11/10			arithmetic, logical
17	M 11/10	***8086 instructions:*** examples on the use of logical instructions. Shift instructions, SHR, SAR, SHL/SAL. **(HW#3 Collected**)	4.1, notes	
18	W 13/10	Review for Exam I**. (Exam I)**		
19	S 16/10	***8086 instructions***: Rotate instructions, ROR, ROL, RCL, RCR. Compare CMP. Conditional jumps, JZ, JNZ, JE, JNE, JS, JNS, JO, JNO, JP, JNP.	3.5, notes	
	M 18/10			shift, rotate, cond. jumps
20	M 18/10	***8086 instructions:*** JMP. Examples of Jumps. **(HW#4 Distributed**)	3.5, notes	
21	W 20/10	***8086 instructions:*** LOOP. Subprograms. CALL, RET.	3.4, notes	
22	S 23/10	***8086 instructions:*** Subprograms and Macros. Stack. The execution of CALL, RET. **(HW#4 Collected**)	3.4, notes	
	M 25/10			loop, subpg.
23	M 25/10	***8086 instructions:*** Stack operations. PUSH, POP. **(Quiz#3)**		
24	W 27/10	***8086 instructions:*** String instructions, MOVSB. I/O instructions, IN, OUT. **(HW#5 Distributed**)	notes	
25	S 30/10	***Computer Structure***: memory hierarchy, random access, access time vs. cycle time, DRAM, SRAM.	5.1, notes	
	M 1/11			Stack, Strings, I/O
26	M 1/11	***Computer Structure***: external memory, disks, direct access, average access time and transfer rate. Tapes, sequential access. CD-ROM. **(HW#5 Collected**)	5.1, notes	
27	W 3/11	***Computer Structure***: I/O controllers and I/O devices. Serial vs. parallel interface. **(Quiz#4)**	5.1, notes	
28	S 6/11	***Computer Structure***: Bus system, data bus, address bus, control bus (command, timing, arbitration). **(HW#6 Distributed**)	5.1, notes	
	M 8/11			Video
29	M 8/11	***Interrupts:*** hardware and software interrupts, INT instruction, interrupt type, interrupt vector table.	Notes	
30	W 10/11	***Interrupts:*** 8086 interrupt processing.	Notes,	

		Introduction to CPU organization.	handout	
31	S 13/11	***CPU Organization:*** 1-bus, 2-bus, and 3-bus organization.	handout	
	M 15/11			
32	M 15/11	***CPU Organization:*** control signals for register transfer, ALU operations, and memory read/write. **(HW#6 Collected**)	handout	
33	W 17/11	Review for Exam II. **(Exam II)**		
34	S 20/11	***CPU Organization:*** Control steps. Fetch phase, read from synchronous and asynchronous memory.	handout	
	M 22/11			Project
35	M 22/11	***CPU Organization:*** control steps examples - fetch and execute phases. **(HW#7 Distributed**)	handout	
36	W 24/11	***CPU Organization:*** control steps –jump instructions (conditional and unconditional).		
37	S 27/11	***CPU Organization:*** CU organization, hardwired vs. microprogrammed. **(HW#7 Collected**)	handout	
	M 29/11			Project
38	M 29/11	***CPU Organization:*** hardwired control unit organization and design. **(Quiz#5)**	handout	
39	W 1/12	***CPU Organization:*** hardwired control unit organization and design.	handout	
40	S 4/12	***CPU Organization:*** microprogrammed control unit organization. Horizontal design. **(HW#8 Distributed**)	handout	
	M 6/12			Project
41	M 6/12	***CPU Organization:*** microprogrammed CU, grouping signals.	handout	
42	W 8/12	***CPU Organization:*** microprogrammed CU , control steps.	handout	
43	S 11/12	***CPU Organization:*** microprogrammed CU, sharing microinstructions, next-address field. **(HW#8 Collected**)	handout, notes	
44	M 13/12	***CPU Organization:*** microprogrammed CU organization. **(Quiz#6)**	handout	
45	W 15/12	Review for Final Exam.		