KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 011 Lectures

	Date	Topics	Ref.	Lab
1	M 3/9	Syllabus. Introduction.	Handout, Chapter 1	
2	W 5/9	The general purpose machine. Views of the computer: the user`s view, the machine/assembly language programmer`s view, the computer architect`s view. Instruction Set Architecture.	Handout, Chapter 1	
3	S 8/9	***Computer structure***: CPU organization, memory organization, and I/O. ***Info. Representation***: Binary, Octal, Hex., representation of signed numbers.	Chapter 2	
	S 8/9			Introduction, using MASM
4	M 10/9	***Info. Representation***: sign-magnitude, 1`s complemet, 2` complement arithmetic, range.	Chapter 2	
5	W 12/9	Overflow, ASCII characters. ***Assembly Concepts***: Assembly language syntax, variables, directives and instructions.	Chapter 4	
6	S 15/9	***Assembly Concepts***: declaring variables (DB, DW, DD), constants (EQU), and arrays (DUP), type and size of information. 8086 memory.	Chapter 4	
	S 15/9			Introduction to IBM PC Assembly Language
7	M 17/9	***8086 registers and memory segmentation:*** list of 8086 registers and their use. Code, data, and stack segments. Offset address and physical address. LEA inst.	Chapter 3	
8	W 19/9	***Assembly Concepts:*** I/O using DOS. INT 21H with functions 1, 2, 8, 9, and A. OFFSET operator.	Chapter 4	
9	S 22/9	***8086 Status and FLAGS Register:*** (Carry, Zero, Sign, Overflow, Parity, Auxiliary).	Chapter 5	
	S 22/9			Input/Output
10	M 24/9	***Addressing Modes:*** register, immediate, direct,	Chapter 10	

		register indirect, Based, Indexed, and Based-Indexed. The PTR operator.		
11	W 26/9	***8086 instructions***: Instruction types, MOV instruction. Data type, accessing memory.	Chapter 4	
12	S 29/9	***8086 instructions***: MOV with indexing, XCHG, ADD, SUB.	Chapter 4	
	S 29/9			Segmentation & addressing modes
13	M 1/10	***8086 instructions***: ADC, SBB, INC, DEC, NEG, CMP.	Chapter 4, Chapter 18	
14	W 3/10	***8086 instructions:*** Multiplication instructions: MUL, IMUL.	Chapter 9	
15	S 6/10	***8086 instructions:*** Division instructions: DIV, IDIV. Sign-extension: CBW, CWD	Chapter 9	
	S 6/10			Indexing, data manipulation
16	M 8/10	***8086 instructions:*** Logic instructions: AND, OR, XOR, NOT, TEST.	Chapter 7	
17	W 10/10	***8086 instructions:*** Shift instructions, SHR, SAR, SHL/SAL. Multiplication/division using shift instructions.	Chapter 7	
18	S 13/10	***8086 instructions***: Rotate instructions, ROR, ROL, RCL, RCR.	Chapter 7	
	S 13/10			Arithmetic, logic instructions
19	M 15/10	***8086 instructions***: Flow control instructions: JMP, conditional jumps, signed and unsigned instructions, JZ, JNZ, JE, JNE, JS, JNS, JO, JNO, JP, JNP.	Chapter 6	
20	W 17/10	***8086 instructions:*** LOOP, LOOPE, LOOPNE, High-level language structures: IF-Then, IF-Then-Else, CASE, FOR LOOP, WHILE LOOP, REPEAT LOOP.	Chapter 6	
21	S 20/10	***8086 instructions:*** Stack operations: PUSH, POP, PUSHF, POPF. Introduction to procedures.	Chapter 8	
	S 20/10			Shift, rotate, jump, loop
22	M 22/10	***8086 instructions:*** The execution of CALL, RET. Parameter passing in subroutines. NEAR and FAR procedures. EXTERN and PUBLIC pseudo-ops.	Chapter 14	
23	W 24/10	***8086 instructions:*** MACROS: definition and	Chapter 13	

		invocation, local labels, macro library.		
24	S 27/10	***8086 instructions:*** Repetition macros, conditionals.	Chapter 13	
	S 27/10			Subroutines & macros
25	M 29/10	***8086 instructions:*** String instructions, Direction flag: CLD, STD, Moving a string: MOVS, MOVSB, MOVSW. The REP prefix.	Chapter 11	
26	W 31/10	***8086 instructions:*** Other string instructions: SCAS, CMPS, LODS, STOS. The REPE, REPNE prefixes.	Chapter 11	
27	S 3/11	***I/O instructions:*** I/O space vs. Memory space, IN, OUT instructions, direct/indirect I/O. ***Interrupts:*** hardware and software interrupts, INT, IRET instructions, interrupt type, interrupt vector table.	Handout, Chapter 15	
	S 3/11			String instructions
28	M 5/11	***Interrupts:*** 8086 interrupt processing. Interrupt examples.	Handout, Chapter 15	
29	W 7/11	***Computer Structure***: Bus system, data bus, address bus, control bus (command, timing, arbitration).	Handout	
30	S 10/11	***Computer Structure***: Memory system design, memory hierarchy, performance parameters, random access, access time vs. cycle time, RAM structure, 1-D and 2-D RAMs.	Handout	
	S 10/11			Interrupts
31	M 12/11	***Computer Structure***: Memory cells, SRAM and DRAM. External memory, disks, direct access, average access time and transfer rate.	Handout	
32	W 14/11	Tapes, sequential access. CD-ROM **.** ***Processor Design***: register transfer, fetch-execute cycle.	Handout	
33	S 17/11	Single-bus CPU. Register transfer timing.	Handout	
	S 17/11			Video memory
34	M 19/11	***Memory-CPU interface:*** Synchronous vs. Asynchronous.	Handout	
35	W 21/11	Execution of add instruction, execution of unconditional and conditional branch instructions.	Handout	
36	S 24/11	***Performance considerations:*** 2-bus CPU & 3-bus CPU.	Handout	
	S 24/11			Using the mouse

37	M 26/11	***Control unit design:*** hardwired control unit organization, generation of control signals.	Handout	
38	W 28/11	CPU-Memory interaction circuit design, practical aspects of circuit implementation.	Handout	
39	S 1/12	Microprogrammed control: microprogrammed control unit operation, microroutines for add & branch on negative.	Handout	
	S 1/12			Project
40	M 3/12	Microprogramed control unit with conditional branching, Microinstruction format: field-encoded.	Handout	
41	W 5/12	Horizontal vs. Vertical control store, Nanocoding, Microcode branching example.	Handout	
42	S 8/12	Microprogram Example: Add instruction with addressing modes.	Handout	
43	S 29/12	Microinstruction sharing, multiway branching, wide branch addressing, Bit Oring.	Handout	
	S 29/12			Project
44	M 31/12	Microinstruction sequencing, Microinstruction format: Example, Control signal generation. Improving performance of microprogrammed control unit.	Handout	
45	W 2/1	Final Exam Review		