KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 003 Lectures

	Date	Topics	Ref.	Lab
1	U 24/6	Syllabus. Introduction. The general purpose machine, Views of the computer: the user`s view, the machine/assembly language programmer`s view, the computer architect`s view.	Handout, Chapter 1	
2	M 25/6	***Computer structure***: Instruction Set Architecture, CPU organization, memory organization, and I/O.	Handout, Chapter 1	
	M 25/6			Introduction, using MASM
3	T 26/6	***Info. Representation***: Binary, Octal, Hex., 2`s complement representation. 2`s complement addition/subtraction, range.	Chapter 2	
4	W 27/6	***Assembly Concepts***: Overflow, ASCII characters, assembly directives and instructions.	Chapter 2	
5	TH 28/6	***Assembly Concepts***: declaring variables (DB, DW, DD), constants (EQU), and arrays (DUP), type and size of information. 8086 memory.	Chapter 4	
6	S 30/6	***Assembly Concepts:*** Assembly instruction format. I/O using DOS functions. INT 21H with functions 1, 2, 8, 9, and A. OFFSET operator.	Chapter 4	
	S 30/6			I/O
7	U 1/7	***8086 registers and memory segmentation:*** list of 8086 registers and their use. Code, data, and stack segments. Offset address and physical address. LEA inst.	Chapter 3	
8	M 2/7	***8086*** Flags (Carry, Zero, Sign, Overflow, Parity, Auxiliary). ***Assembly Concepts:*** Addressing modes.	Chapter 5, 10	
	M 2/7			Segmentation & addressing modes
9	T 3/7	***Assembly Concepts:*** Addressing modes. Instruction types, MOV instruction. Data type, accessing memory.	Chapter 4, 10	
10	W 4/7	***8086 instructions***: MOV with indexing, XCHG, ADD, SUB, ADC, SBB, INC, DEC.	Chapter 4, Chapter 18	
11	S 7/7	***8086 instructions***: NEG, CMP, CBW, CWD, MUL, IMUL	Chapter 9	
	S 7/7			Indexing, data manipulation

12	U 8/7	***8086 instructions:*** DIV, IDIV	Chapter 9	
13	M 9/7	***8086 instructions:*** Logical instructions, AND, OR, XOR, NOT, TEST.	Chapter 7	
	M 9/7			Arithmetic, logical
14	T 10/7	***8086 instructions:*** Shift instructions, SHR, SAR, SHL/SAL.	Chapter 7	
15	W 11/7	***8086 instructions***: Rotate instructions, ROR, ROL, RCL, RCR.	Chapter 7	
16	S 14/7	***8086 instructions:*** Jump instructions. Conditional jumps, JZ, JNZ, JE, JNE, JS, JNS, JO, JNO, JP, JNP.	Chapter 5	
	S 14/7			Shift, rotate, jump, loop
17	U 15/7	***8086 instructions:*** Conditional jumps: signed and unsigned instructions. LOOP, LOOPE, LOOPNE.	Chapter 5	
18	M 16/7	***8086 instructions:*** Stack operations: PUSH, POP. Subprograms and Macros. The execution of CALL, RET.	Chapter 8, 13	
	M 16/7			Subroutines & macros
19	T 17/7	***8086 instructions:*** Parameter passing in subroutines and macros.	Chapter 13, 14	
20	W 18/7	***8086 instructions:*** String instructions, CLD, STD, MOVS.	Chapter 11	
21	S 21/7	***8086 instructions:*** SCAS, CMPS, LODS, STOS, SCAS String instructions prefixes: REP, REPE, REPNE.	Chapter 11	
	S 21/7			String instructions
22	U 22/7	I/O instructions, IN, OUT. ***Interrupts:*** hardware and software interrupts, INT instruction, interrupt type, interrupt vector table.	Handout, Chapter 15	
23	M 23/7	***Interrupts:*** 8086 interrupt processing.	Handout, Chapter 15	
	M 23/7			Interrupts
24	T 24/7	***Computer Structure***: Bus system, data bus, address bus, control bus (command, timing, arbitration).	Handout	
25	W 25/7	***Computer Structure***: memory hierarchy, random access, access time vs. cycle time, DRAM, SRAM.	Handout	
26	S 28/7	***Computer Structure***: external memory, disks, direct access, average access time and transfer rate. Tapes, sequential access. CD-ROM.	Handout	
27	U 29/7	Processor Design: Datapath and Control unit, register transfer, fetch-execute cycle.	Handout	
28	M 30/7	Single-bus CPU. Register transfer timing.	Handout	
	M 30/7			Video

				memory
29	T 31/7	***Memory-CPU interface:*** Synchronous vs. Asynchronous.	Handout	
30	W 1/8	Single-Bus CPU: Execution of add instruction, execution of unconditional and conditional branch instructions.	Handout	
31	S 4/8	***Performance considerations:*** 2-bus CPU & 3-bus CPU.	Handout	
	S 4/8			Using the mouse
32	U 5/8	***Control unit design:*** hardwired control unit organization, generation of control signals.	Handout	
33	M 6/8	CPU-Memory interaction circuit design, practical aspects of circuit implementation. ***An example of a simple CPU design.***	Handout	
	M 6/8			Serial Communication
34	T 7/8	Microprogrammed control: microprogrammed control unit operation, microroutines for add & branch on negative.	Handout	
35	W 8/8	Microprogrammed control: microprogramed control unit with conditional branching, microinstruction format:field-encoded.	Handout	
36	S 11/8	Horizontal vs. Vertical control store, Nanocoding, Microcode branching example. ***Microprogram Example***: Add instruction with addressing modes.	Handout	
	S 11/8			Lab Exam
37	U 12/8	Microinstruction sharing, multiway branching, wide branch addressing, Bit Oring.	Handout	
38	M 13/8	Microinstruction sequencing, Microinstruction format:Example, Control signal generation. Improving performance of microprogrammed control unit.	Handout	