KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 001 Lectures

	Date	Topics	Ref.	Lab
1	M 4/9	Syllabus. Introduction.	Handout	
2	W 6/9	The general purpose machine. Views of the computer: the user`s view, the machine/assembly language programmer`s view, the computer architect`s view. Instruction Set Architecture.	Handout	
3	S 9/9	***Computer structure***: CPU organization, memory organization, and I/O. ***Info. Representation***: Binary, Octal, Hex., representation of signed numbers.	2.2, Handout App. B	
	S 9/9			Introduction, using MASM
4	M 11/9	***Info. Representation***: sign-magnitude, 1`s complemet, 2` complement arithmetic, range.	App. B	
5	W 13/9	Overflow, ASCII characters. ***Assembly Concepts***: Assembly language syntax, variables, directives and instructions.	2.1, 2.3	
6	S 16/9	***Assembly Concepts***: declaring variables (DB, DW, DD), constants (EQU), and arrays (DUP), type and size of information. 8086 memory.	2.3, 2.5, handout	
	S 16/9			Introduction to IBM PC Assembly Language
7	M 18/9	***8086 registers and memory segmentation:*** list of 8086 registers and their use. Code, data, and stack segments. Offset address and physical address. LEA inst.	3.1, 3.2 handout	
8	W 20/9	***Assembly Concepts:*** I/O using DOS. INT 21H with functions 1, 2, 8, 9, and A. OFFSET operator.	3.3	
9	S 23/9	***8086 Status and FLAGS Register:*** (Carry, Zero, Sign, Overflow, Parity, Auxiliary).	3.1, 4.3, handout	
	S 23/9			Input/Output
10	M 25/9	***Addressing Modes:*** register, immediate, direct, register indirect, Based, Indexed, and Based-Indexed. The PTR operator.	4.3, handout	

11	W 27/9	***8086 instructions***: Instruction types, MOV instruction. Data type, accessing memory.	3.2, handout	
12	S 30/9	***8086 instructions***: MOV with indexing, XCHG, ADD, SUB.	3.2, handout	
	S 30/9			Segmentation & addressing modes
13	M 2/10	***8086 instructions***: ADC, SBB, INC, DEC, NEG, CMP.	3.2, handout	
14	W 4/10	***8086 instructions:*** Multiplication instructions: MUL, IMUL.	3.2, handout	
15	S 7/10	***8086 instructions:*** Division instructions: DIV, IDIV. Sign-extension: CBW, CWD	3.2, handout	
	S 7/10			Indexing, data manipulation
16	M 9/10	***8086 instructions:*** Logic instructions: AND, OR, XOR, NOT, TEST.	4.1, handout	
17	W 11/10	***8086 instructions:*** Shift instructions, SHR, SAR, SHL/SAL. Multiplication/division using shift instructions.	4.1, handout	
18	S 14/10	***8086 instructions***: Rotate instructions, ROR, ROL, RCL, RCR. **(EXAM I)**	4.1, handout	
	S 14/10			Arithmetic, logic instructions
19	M 16/10	***8086 instructions***: Flow control instructions: JMP, conditional jumps, signed and unsigned instructions, JZ, JNZ, JE, JNE, JS, JNS, JO, JNO, JP, JNP.	3.5, handout	
20	W 18/10	***8086 instructions:*** LOOP, LOOPE, LOOPNE, High-level language structures: IF-Then, IF-Then-Else, CASE, FOR LOOP, WHILE LOOP, REPEAT LOOP.	3.5, handout	
21	S 21/10	***8086 instructions:*** Stack operations: PUSH, POP, PUSHF, POPF. Introduction to procedures.	2.4, handout	
22	U 22/10	***8086 instructions:*** The execution of CALL, RET. Parameter passing in subroutines. NEAR and FAR procedures. EXTERN and PUBLIC pseudo-ops.	3.4, 4.4 handout	
23	S 28/10	***8086 instructions:*** MACROS: definition and invocation, local labels, macro library.	4.2, handout	
	S 28/10			Shift, rotate, jump, loop
24	M 30/10	***8086 instructions:*** Repetition macros, conditionals.	Handout	

25	W 1/11	***8086 instructions:*** String instructions, Direction flag: CLD, STD, Moving a string: MOVS, MOVSB, MOVSW. The REP prefix.	Handout	
26	S 4/11	***8086 instructions:*** Other string instructions: SCAS, CMPS, LODS, STOS. The REPE, REPNE prefixes.	Handout	
	S 4/11			Subroutines & macros
27	M 6/11	***I/O instructions:*** I/O space vs. Memory space, IN, OUT instructions, direct/indirect I/O. ***Interrupts:*** hardware and software interrupts, INT, IRET instructions, interrupt type, interrupt vector table.	Handout	
28	W 8/11	***Interrupts:*** 8086 interrupt processing. Interrupt examples.	5.1, handout	
29	S 11/11	***Computer Structure***: Bus system, data bus, address bus, control bus (command, timing, arbitration).	5.1, handout	
	S 11/11			String instructions
30	M 13/11	***Computer Structure***: Memory system design, memory hierarchy, performance parameters, random access, access time vs. cycle time, RAM structure, 1-D and 2-D RAMs. **(EXAM II).**	5.1, handout	
31	W 15/11	***Computer Structure***: Memory cells, SRAM and DRAM. External memory, disks, direct access, average access time and transfer rate.	5.1, handout	
32	S 18/11	Tapes, sequential access. CD-ROM **.** ***Processor Design***: register transfer, fetch-execute cycle.	5.1, handout	
	S 18/11			Interrupts
33	M 20/11	Single-bus CPU. Register transfer timing.	Handout	
34	W 22/11	***Memory-CPU interface:*** Synchronous vs. Asynchronous.	Handout	
35	S 25/11	Execution of add instruction, execution of unconditional and conditional branch instructions.	Handout	
	S 25/11			Video memory
36	M 27/11	***Performance considerations:*** 2-bus CPU & 3-bus CPU.	Handout	
37	W 29/11	***Control unit design:*** hardwired control unit organization, generation of control signals.	Handout	
38	S 2/12	CPU-Memory interaction circuit design, practical aspects of circuit implementation.	Handout	
	S 2/12			Using the mouse
39	M 4/12	Microprogrammed control: microprogrammed	Handout	

		control unit operation, microroutines for add & branch on negative.		
40	W 6/12	Microprogramed control unit with conditional branching, Microinstruction format: field-encoded.	Handout	
41	S 9/12	Horizontal vs. Vertical control store, Nanocoding, Microcode branching example.	Handout	
	S 9/12			Project
42	M 11/12	Microprogram Example: Add instruction with addressing modes.	Handout	
43	W 13/12	Microinstruction sharing, multiway branching, wide branch addressing, Bit Oring.	Handout	
44	M 1/1	Microinstruction sequencing, Microinstruction format: Example, Control signal generation. Improving performance of microprogrammed control unit.	Handout	
45	W 3/1	Final Exam Review		