

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 101 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	S 25/9	No Class.	
2	M 27/9	Course Introduction, Assembly and machine language. Compiler and assembler. Instruction and machine language, Instruction fields: opcode, operands, Assembly vs. Machine code, Translating languages.	Chapter1 & Int. Computer Org. & Assembly Lang. Prog. (Online)
3	W 29/9	Advantages of High-Level languages, Why learn Assembly language? Assembly vs. High-level languages. Assembly language programming tools: Assembler, Linker, Debugger, Editor. Programmer's view of a computer system. Instruction set architecture. I-8086 instruction set architecture. Basic Computer Organization, Processor. Processor, Clock, Memory.	Chapter1 & 2 & Int. Computer Org. & Assembly Lang. Prog. (Online)
4	S 2/10	Memory, Address Space, Address, Data, and Control Bus, Memory Devices: RAM. Static vs. Dynamic RAM. Processor-Memory Performance Gap, Memory Hierarchy: Registers, RAM, Cache, Hard disk.	Chapter1 & 2 & Int. Computer Org. & Assembly Lang. Prog. (Online)
5	M 4/10	Magnetic Disk Storage access time. Review of data representation.	Chapter1 & 2 & Int. Computer Org. & Assembly Lang. Prog. (Online)
6	W 6/10	Review of data representation. History of Intel Processors. Intel Core MicroArchitecture, CISC vs. RISC processors.	Chapter1 & 2 & Int. Computer Org. & Assembly Lang. Prog. (Online)
7	S 9/10	IA-32 Registers. Status Flags: CF, AF, ZF, SF, PF, OF. (Quiz#1)	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
8	M 11/10	Status Flags: CF, AF, ZF, SF, PF, OF. Fetch-Execute cycle. Pipelined Execution.	Chapter 2 & Int. Computer Org. and Assembly Lang.

			Prog. (Online)
9	W 13/10	Pipelined Execution. Superscalar Architecture, IA-32 Memory Management, Modes of Operation, Real Address Mode: Logical to Linear Address Translation. Flat Memory Model. Protected Mode Architecture and address translation.	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
10	S 16/10	Protected Mode Architecture and address translation, Segment Descriptor Tables, Paging. Basic Elements of Assembly Language, Flat Memory Program Template, Assembling, Linking, and Debugging Programs. Variable Declaration: DB, BYTE, SBYTE.	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
11	M 18/10	Variable Declaration: DB, BYTE, SBYTE, DW, WORD, SWORD, DD, DWORD, SDWORD, DQ, QWORD, DT, TBYTE. Defining strings. DUP Operator. Byte Ordering. Defining Symbolic Constants: =, EQU & TEXTEQU Directives. Offset Operator.	Chapter 3 & Variable, Constant, and Array Declaration (Online)
12	W 20/10	Align Directive. Type, Lengthof, Sizeof, PTR operators. (Quiz#2)	Chapter 3 & Variable, Constant, and Array Declaration (Online)
13	S 23/10	PTR operators. Label directive. Operand Types. Basic Pentium Instructions: MOV, MOVZX, MOVSX, XCHG.	Chapter 4 & (Assembly) Basic Pentium Instructions (Online)
	S 23/10 (Makeup)	Direct Memory Operands, Direct-Offset Operands. ADD and SUB instructions and their effect on flags.	Chapter 4 & (Assembly) Basic Pentium Instructions (Online)
14	M 25/10	INC, DEC, NEG, ADC, SBB. Addressing Modes: Immediate, Register, Direct, Register Indirect, Indexed.	Chapter 4 & (Assembly) Basic Pentium Instructions (Online)
15	W 27/10	Addressing modes: Based, Indexed, Based-Indexed. 8086 Addressing modes. Two dimensional array processing. Default segments and Segment Override. LEA instruction. JMP instruction.	Chapter 4 (Assembly) & Addressing Modes (Online)
	Th. 28/10	Major Exam I	
16	S 30/10	No Class.	
17	M 1/11	JMP and Loop instructions. Nested Loops. Example Programs: Copying a string, Summing an Array.	Chapter 4 (Assembly) & Addressing Modes (Online)

18	W 3/11	PC relative addressing, Link Library Overview, Calling a Library Procedure, Linking to a Library, Input/Output procedures using book's library (Irvine32.lib).	Chapter 4 & 5 (Assembly) & Addressing Modes (Online)
	W 3/11	Last Day for Dropping with W	
19	S 6/11	Introduction to Stack. Stack instructions: Push and Pop. Uses of the Runtime Stack: Temporary Storage of Registers, Nested Loop.	Chapter 5 (Assembly) & Stack & Procedures (Online)
	U 7/11 (Makeup)	Stack Instructions: pushad, pusha, popad, popa, pushfd, pushf, popfd, popf. Defining and Using Procedures , Call & RET Instructions. Parameter Passing, Passing Parameters in Registers. Preserving Registers, USES Operator. Parameter Passing Through Stack. Call & Return Instructions.	Chapter 5 (Assembly) & Stack & Procedures (Online)
20	M 8/11	Parameter Passing Through Stack, Call & RET Instructions. Defining and using Local variables, Stack Frame, Program Design using Procedures, Integer Summation Program. Example of a Recursive Procedure: Factorial.	Chapter 5 (Assembly) & Stack & Procedures (Online)
21	W 10/11	Logical Instructions: AND. (Quiz#3)	
	11-26/11	Eid Al-Adha Vacation	
22	S 27/11	Logical Instructions: AND, OR, XOR, Test, NOT. Applications of logic instructions. Flow Control Instructions: CMP Instruction. Conditional Jump instructions: Signed and Unsigned. Conditional Jump instructions: Single-flag jump instructions. Jumps Based on Equality.	Chapter 6 (Assembly) & Flow Control Instructions (Online)
23	M 29/11	Jumps Based on Unsigned Comparison, Jumps Based on Signed Comparisons. BT Instruction, Conditional Loop Instructions: Loope/Loopz, Loopne/Loopnz. High-Level Decision Control Structures: IF-Then-Else.	Chapter 6 (Assembly) & Flow Control Instructions (Online)
24	W 1/12	Compound Expression with AND, Compound Expression with OR, WHILE Loop, Do While Loop, For Loop, Indirect Jump, Switch Statement. Bubble Sort Algorithm.	Chapter 6 (Assembly) & Flow Control Instructions (Online)
25	S 4/12	Bubble Sort Algorithm. Shift Instructions: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication & division.	Chapter 7 (Assembly) & Bit Manipulation Instructions (Online)

26	M 6/12	Rotate Instructions: ROL, ROR, RCL, RCR. (Quiz#4)	Chapter7 (Assembly) & Bit Manipulation Instructions (Online)
27	W 8/12	SHLD instruction. SHRD instructions. Shift & Rotate Applications.	Chapter7 (Assembly) & Bit Manipulation Instructions (Online)
28	S 11/12	Shift & Rotate Applications. Multiplication Instructions: MUL, IMUL. Pentium IMUL instructions. Division Instructions: DIV, IDIV. Sign Extension Instructions: CBW, CWD, CDQ.	Chapter7 (Assembly) & Advanced Arithmetic (Online)
	U 12/12	Last Day for Dropping all Courses with W	
29	M 13/12	Translating Arithmetic Expressions, Decimal string to number conversions. Number to decimal string conversion. Review for Major Exam II.	Chapter7 (Assembly) & Advanced Arithmetic (Online)
30	W 15/12	CPU Design: Register Transfer. (Quiz#5)	CPU Design (Online)
31	S 18/12	Data-Path Design. Connecting Registers using Muxs, Connecting Registers using a tri-state bus.	CPU Design (Online)
	S 18/12	Major Exam II	
32	M 20/12	Data Path Design for implementing ADD, SUB, INC, DEC and Shift Instructions. Register Transfer Timing. Single-Bus CPU Data path design: Fetch Control Sequence.	CPU Design (Online)
33	W 22/12	Fetch Control Sequence. Synchronous vs. Asynchronous Memory Transfer. Execution control sequence for ADD with register indirect addressing mode. Execution control sequence for unconditional JMP, Conditional JMP. Execution control sequence for ADD R1, 2, INC [R1], CMP, Loop, PUSH.	CPU Design (Online)
34	S 25/12	Performance Considerations. Two-Bus CPU: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump.	CPU Design (Online)
35	M 27/12	Three-Bus CPU. Fetch Control Sequence, Execution Control Sequence for ADD. Unconditional and Conditional Jump Instructions. Control Unit Design:	CPU Design (Online)

		Hardwired Control Unit, General Hardwired Control Unit Organization, Generation of Control Signals.	
36	W 29/12	No Class.	
37	S 1/1	(Quiz#6)	
38	M 3/1	Deriving Rout & Rin Signals. CPU-Memory Interface Circuit.	CPU Design (Online)
39	W 5/1	CPU-Memory Interface Circuit. Microprogrammed Control Unit Design: Control Word, Control Store, Micro Program Counter, Micro Instruction Register.	CPU Design (Online)
40	S 8/1	Microprogrammed Control Unit Design: Microinstruction, Microroutine. General Organization of Micro-programmed Control Unit, Branching Address, Sequencer. Horizontal, and field-encoded microprogramming.	CPU Design (Online)
	U 9/1	Dropping all Courses with WP/WF	
41	M 10/1	Horizontal, vertical and field-encoded microprogramming. Simple CPU Design Example.	CPU Design (Online)
42	W 12/1	Simple CPU Design Example. Introduction to Interrupts. Interrupts vs. procedures. Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag.	Interrupts (Online)
43	S 15/1	Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag. Interrupt Processing, IDT, IRET, Dedicated Interrupts.	Interrupts (Online)
44	M 17/1	Final Exam Review.	
45	W 19/1	Final Exam Review.	