KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 205 Computer Organization & Assembly Language

**Term 092 Lecture Breakdown**

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | S 20/2 | Course Introduction. |  |
| 2 | M 22/2 | Assembly and machine language. Compiler and assembler. Instruction and machine language, Instruction fields: opcode, operands, Assembly vs. Machine code, Translating languages. Advantages of High-Level languages, Why learn Assembly language? | Chapter1 &  Int. Computer Org. & Assembly Lang. Prog.  (Online) |
| 3 | W 24/2 | Assembly vs. High-level languages. Assembly language programming tools: Assembler, Linker, Debugger, Editor. Programmer’s view of a computer system. Instruction set architecture. I-8086 instruction set architecture. | Chapter1 &  Int. Computer Org. & Assembly Lang. Prog.  (Online) |
| 4 | S 27/2 | Basic Computer Organization, Processor. Processor, Clock, Memory, Address Space,  Address, Data, and Control Bus, Memory Read and Write Cycles, Memory Devices: RAM. Static vs. Dynamic RAM. | Chapter1 & 2 &  Int. Computer Org. & Assembly Lang. Prog.  (Online) |
| 5 | M 1/3 | Processor-Memory Performance Gap, Memory Hierarchy: Registers, RAM, Cache, Hard disk. Magnetic Disk Storage access time. History of Intel Processors. Intel Core MicroArchitecture, CISC vs. RISC processors. | Chapter1 & 2 &  Int. Computer Org. & Assembly Lang. Prog.  (Online) |
| 6 | W 3/3 | IA-32 Registers. Status Flags: CF, AF, ZF, SF, PF, OF. Fetch-Execute cycle. | Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online) |
| 7 | S 6/3 | Pipelined Execution. Superscalar Architecture, IA-32 Memory Management, Modes of Operation, Real Address Mode: Logical to Linear Address Translation. **(Quiz#1)** | Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online) |
| 8 | M 8/3 | Flat Memory Model. Protected Mode Architecture and address translation, Segment Descriptor Tables, Paging. | Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online) |
| 9 | W 10/3 | Basic Elements of Assembly Language, Flat Memory Program Template, Assembling, Linking, and Debugging Programs. **Variable Declaration**: DB, BYTE, SBYTE, DW, WORD, SWORD, DD, DWORD, SDWORD, DQ, QWORD, DT, TBYTE. Defining strings. DUP Operator. Byte Ordering. | Chapter 3 &  Variable, Constant, and Array Declaration (Online) |
| 10 | S 13/3 | **Variable Declaration**: DW, WORD, SWORD, DD, DWORD, SDWORD, DQ, QWORD, DT, TBYTE. Byte Ordering. **(Quiz#2)** | Chapter 3 &  Variable, Constant, and Array Declaration (Online) |
| 11 | M 15/3 | Defining Symbolic Constants: =, EQU & TEXTEQU Directives. Offset Operator, Align Directive. Type, Lengthof, Sizeof, PTR operators. Label directive. | Chapter 3 &  Variable, Constant, and Array Declaration (Online) |
| 12 | W 17/3 | Operand Types. **Basic Pentium Instructions**: MOV, MOVZX, MOVSX, XCHG. Direct Memory Operands, Direct-Offset Operands. | Chapter 4 &  (Assembly)  Basic Pentium Instructions (Online) |
| 13 | S 20/3 | ADD and SUB instructions and their effect on flags. **(Quiz#3)** | Chapter 4 &  (Assembly)  Basic Pentium Instructions (Online) |
| 14 | M 22/3 | INC, DEC, NEG, ADC, SBB. Addressing Modes: Immediate, Register, Direct, Register Indirect. | Chapter 4 &  (Assembly)  Basic Pentium Instructions (Online) |
| 15 | W 24/3 | Addressing modes: Based, Indexed, Based-  Indexed. 8086 Addressing modes. Two dimensional array processing. Default segments and Segment Override. | Chapter 4  (Assembly)  &Addressing Modes  (Online) |
| 16 | S 27/3 | LEA instruction. JMP and Loop instruction.  Nested Loops. Example Programs: Copying a string, Summing an Array. | Chapter 4  (Assembly)  &Addressing Modes  (Online) |
|  | S 27/3 | **Major Exam I** |  |
| 17 | M 29/3 | PC relative addressing. Link Library Overview, Calling a Library Procedure, Linking to a Library, Input/Output procedures using book’s library (Irvine32.lib). | Chapter 4 & 5  (Assembly)  &Addressing Modes  (Online) |
| 18 | W 31/3 | Input/Output procedures using book’s library (Irvine32.lib). | Chapter 5  (Assembly)  &Addressing Modes  (Online) |
|  | W 31/3 | **Last Day for Dropping with W** |  |
| 19 | S 3/4 | **Introduction to Stack. Stack instructions**: Push and Pop. Uses of the Runtime Stack: Temporary Storage of Registers. | Chapter 5  (Assembly) &  Stack & Procedures  (Online) |
| 20 | M 5/4 | Nested Loop, Saving Return Address. Stack Instructions: pushad, pusha, popad, popa, pushfd, pushf, popfd, popf. **Defining and Using Procedures**, Call & RET Instructions. Parameter Passing, Passing Parameters in Registers. Preserving Registers, USES Operator. Parameter Passing Through Stack. Call & Return Instructions. | Chapter 5  (Assembly) &  Stack & Procedures (Online) |
| 21 | W 7/4 | No Class. |  |
| 22 | S 10/4 | Call & RET Instructions. Program Design using Procedures, Integer Summation Program. | Chapter 5  (Assembly) &  Stack & Procedures (Online) |
| 23 | M 12/4 | Integer Summation Program, Example of a Recursive Procedure: Factorial. **Logical Instructions**: AND, OR, XOR. | Chapter 5  (Assembly) &  Stack & Procedures (Online) |
|  | T 13/4 (Makeup) | Test, NOT. Applications of logic instructions. **Flow Control Instructions**: CMP Instruction. Conditional Jump instructions: Signed and Unsigned. Conditional Jump instructions: Single-flag jump instructions. Jumps Based on Equality, Jumps Based on Unsigned Comparison, Jumps Based on Signed Comparisons. | Chapter 6  (Assembly)  & Flow Control Instructions  (Online) |
| 24 | W 14/4 | BT Instruction, Conditional Loop Instructions: Loope/Loopz, Loopne/Loopnz.High-Level Decision Control Structures: IF-Then-Else. Compound Expression with AND. | Chapter 6  (Assembly)  & Flow Control Instructions  (Online) |
|  | 17/4-21/4 | **Midterm Vacation** |  |
| 25 | S 24/4 | Compound Expression with OR, WHILE Loops, Indirect Jump, Switch Statement. Bubble Sort Algorithm. | Chapter 6  (Assembly)  & Flow Control Instructions  (Online) |
| 26 | M 26/4 | **(Quiz#4)** |  |
| 27 | W 28/4 | **Shift Instructions**: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication & division. **Rotate Instructions**: ROL, ROR, RCL, RCR. | Chapter7  (Assembly)  & Bit Manipulation Instructions  (Online) |
| 28 | S 1/5 | SHLD instruction. SHRD instructions. Shift & Rotate Applications. | Chapter7  (Assembly)  & Bit Manipulation Instructions  (Online) |
| 29 | M 3/5 | Shift & Rotate Applications. **Multiplication Instructions**: MUL, IMUL. Pentium IMUL instructions. **Division Instructions**: DIV. | Chapter7  (Assembly)  & Advanced Arithmetic  (Online) |
| 30 | W 5/5 | **Division Instructions**: IDIV. Sign Extension Instructions: CBW, CWD, CDQ. Translating Arithmetic Expressions, Decimal string to number conversions. Number to decimal string conversion. | Chapter7  (Assembly)  & Advanced Arithmetic  (Online) |
|  | W 5/5 | **Last Day for Dropping all Courses with W** |  |
| 31 | S 8/5 | **CPU Design**: Register Transfer. **Data-Path Design**. Connecting Registers using Muxs. | CPU Design (Online) |
| 32 | M 10/5 | **Data-Path Design**. Connecting Registers using a tri-state bus. **(Quiz#5)** | CPU Design (Online) |
|  | T 11/5 (Makeup) | Register Transfer Timing. **Single-Bus CPU Data path design**: Fetch Control Sequence. Synchronous vs. Asynchronous Memory Transfer. | CPU Design (Online) |
| 33 | W 12/5 | Execution control sequence for ADD with register indirect addressing mode. Execution control sequence for unconditional JMP, Conditional JMP. | CPU Design (Online) |
| 34 | S 15/5 | Execution control sequence for INC [R1], CMP, Loop, and Call instructions. Performance Considerations. | CPU Design (Online) |
| 35 | M 17/5 | Performance Considerations. **Two-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump. **(Quiz#6)** | CPU Design (Online) |
| 36 | W 19/5 | **Three-Bus CPU.** Fetch Control Sequence, Execution Control Sequence for ADD. unconditional and conditional Jump Instructions. **Control Unit Design: Hardwired Control Unit,** General Hardwired Control Unit Organization, Generation of Control Signals. | CPU Design (Online) |
|  | Th. 20/5 | **Major Exam II** |  |
| 37 | S 22/5 | Deriving Rout & Rin Signals. **CPU-Memory Interface Circuit.** | CPU Design (Online) |
|  | U 23/5 (Makeup) | **CPU-Memory Interface Circuit. Microprogrammed Control Unit Design*:*** Control Word, Control Store, Micro Program Counter, Micro Instruction Register, Microinstruction, Microroutine. General Organization of Micro-programmed Control Unit, Branching Address, Sequencer. Horizontal, vertical and field-encoded microprogramming. | CPU Design (Online) |
| 38 | M 23/5 | Solution of Major Exam II. |  |
| 39 | W 26/5 | Simple CPU Design Example. | CPU Design (Online) |
| 40 | S 29/5 | No Class. |  |
| 41 | M 31/5 | No Class. |  |
| 42 | W 2/6 | No Class. |  |
|  | W 2/6 | **Dropping all Courses with WP/WF** |  |
| 43 | S 5/6 | **Introduction to Interrupts**. Interrupts vs. procedures.Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag. Interrupt Processing, IDT. | Interrupts (Online) |
| 44 | M 7/6 | Trap Flag, Dedicated Interrupts. **Final Exam Review**. | Interrupts (Online) |
| 45 | W 9/6 | **Final Exam Review. (Quiz#7)** |  |