KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 071 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	S 8/9	Syllabus. Introduction.	
2	M 10/9	Assembly and machine language, Compiler and assembler. Instruction and machine language, Instruction fields: opcode, operands, Assembly vs. Machine code, Translating languages.	Chapter1 & Int. Computer Org. & Assembly Lang. Prog. (Online)
3	W 12/9	Advantages of High-Level languages, Why learn Assembly language, Assembly vs. High-level languages. Assembly language programming tools: Assembler, Linker, Debugger, Editor. Programmer's view of a computer system. Instruction set architecture, Basic Computer Organization, Processor.	Chapter1 & Int. Computer Org. & Assembly Lang. Prog. (Online)
4	S 15/9	Processor, Clock, Memory, Address Space, Address, Data, and Control Bus, Memory Read and Write Cycles, Memory Devices: RAM.	Chapter2 & Int. Computer Org. & Assembly Lang. Prog. (Online)
5	M 17/9	Static vs. Dynamic RAM. Processor-Memory Performance Gap, Memory Hierarchy: Registers, RAM, Cache, Hard disk. Magnetic Disk Storage access time, I/O Devices. Data Representation: Binary Numbers.	Chapter1 & Chapter 2 & Int. Computer Org. & Assembly Lang. Prog. (Online)
6	W 19/9	Hexadecimal Numbers, Base Conversions, Integer Storage Sizes, Binary and, Hexadecimal Addition, Signed Integers.	Chapter1 & Data Representation (Online)
7	S 22/9	Two's complement representation, Sign extension, 16's complement, binary and hexadecimal subtraction, Ranges of signed integers, carry and overflow.	Chapter1 & Data Representation (Online)
8	M 24/9	Character representation: ASCII code, parity bit. **(Quiz#1)**	Chapter1 & Data Representation (Online)
9	W 26/9	Intel Microprocessors: History of processors. CISC vs. RISC processors. IA-32 Registers, Status Flags.	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog.

			(Online)
10	S 29/9 (Ext.)	Fetch-Execute cycle. Pipelined Execution, Superscalar Architecture, IA-32 Memory Management, Modes of Operation, Real Address Mode: Logical to Linear Address Translation.	Chapter 2 & Int. Computer Org. and Assembly Lang. Prog. (Online)
11	M 1/10 (Ext.)	Flat Memory Model, Protected Mode Architecture and address translation, Segment Descriptor Tables, Paging. Basic Elements of Assembly Language	Chapter 2 & 3 Assembly Language Syntax and Program Structure (Online)
12	W 3/10	No Class.	
13	S 20/10	Flat Memory Program Template, Assembling, Linking, and Debugging Programs. **Variable Declaration**: DB, BYTE, SBYTE, DW, WORD, SWORD, DD, DWORD, SDWORD, DQ, QWORD, DT, TBYTE.	Chapter 3 & Variable, Constant, and Array Declaration (Online)
14	M 22/10	Defining strings. DUP Operator. Byte Ordering, Defining Symbolic Constants: =, EQU & TEXTEQU Directives. Offset Operator, Align Directive.	Chapter 3 & Variable, Constant, and Array Declaration (Online)
15	W 24/10	Type, Lengthof, Sizeof , PTR operators. Label directive. Operand Types. **Basic Pentium Instructions**: MOV, MOVZX, MOVSX.	Chapter 4 & (Assembly) Basic Pentium Instructions (Online)
16	S 27/10	**Basic Pentium Instructions**: XCHG. Direct Memory Operands, Direct-Offset Operands**. (Quiz#2)**	Chapter 4 & (Assembly) Basic Pentium Instructions (Online)
17	M 29/10	ADD and SUB instructions and their effect on flags.	Chapter 4 & (Assembly) Basic Pentium Instructions (Online)
18	W 31/10	INC, DEC, NEG, ADC, SBB. JMP & Loop Instruction. Addressing Modes: Immediate, Register, Direct, Register Indirect.	Chapter 4 & (Assembly) Basic Pentium Instructions (Online)
19	S 3/11	Addressing modes: Based, Indexed, Based-Indexed. 8086 Addressing modes. Two-dimensional array processing. LEA instruction.	Chapter 4 (Assembly) &Addressing Modes (Online)
	S 3/11	MAJOR EXAM I	
20	M 5/11	Review of Addressing modes. Default segments and Segment Override. PC relative addressing.	Chapter 4 (Assembly) &Addressing Modes

			(Online)
21	W 7/11	Solution of First Major Exam.	
22	S 10/11	Link Library Overview, Calling a Library Procedure, Linking to a Library, Input/Output procedures using book's library (Irvine32.lib).	Chapter5 (Assembly)
23	M 12/11	Input/Output libraries, **Stack instructions**: Push and Pop.	Chapter5 (Assembly) & Stack & Procedures (Online)
24	W 14/11	**Stack instructions**: Push and Pop. Uses of the Runtime Stack: Temporary Storage of Registers, Nested Loop, Saving Return Address. Stack Instructions: pushad, pusha, popad, popa, pushfd, pushf, popfd, popf.	Chapter5 (Assembly) & Stack & Procedures (Online)
25	S 17/11	**Defining and Using Procedures**, Call & RET Instructions **(Quiz#3).**	Chapter5 (Assembly) & Stack & Procedures (Online)
26	M 19/11	Parameter Passing, Preserving Registers, USES Operator, Program Design using Procedures.	Chapter5 (Assembly) & Stack & Procedures (Online)
27	W 21/11	Parameter Passing Through Stack, Call & Return Instructions, Freeing Passed Parameters From Stack, Local Variables.	Chapter5 (Assembly) & Stack & Procedures (Online)
28	S 24/11	**Logical Instructions**: AND, OR, XOR**,** Test, NOT. Applications of logic instructions. **(Quiz#4).**	Chapter6 (Assembly) & Flow Control Instructions (Online)
29	M 26/11	**Flow Control Instructions**: CMP Instruction. Conditional Jump instructions: Signed and Unsigned. Single-flag jump instructions.	Chapter6 (Assembly) & Flow Control Instructions (Online)
30	W 28/11	Conditional Loop Instructions:Loope/Loopz, Loopne/Loopnz. High-Level Decision Control Structures: IF-Then-Else**,** Compound Expression with AND.	Chapter6 (Assembly) & Flow Control Instructions (Online)
31	S 1/12	Compound Expression with OR, WHILE Loops, For Loops, Indirect Jump, Switch Statement, Bubble Sort Algorithm.	Chapter6 (Assembly) & Flow Control Instructions

			(Online)
32	M 3/12	**Shift Instructions**: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication. Applications of using shift instructions in performing division. **Rotate Instructions**: ROL, ROR, RCL, RCR.	Chapter7 (Assembly) & Bit Manipulation Instructions (Online)
33	W 5/12	SHLD, SHRD instructions. Shift & Rotate Applications.	Chapter7 (Assembly) & Bit Manipulation Instructions (Online)
34	S 8/12	**Multiplication Instructions**: MUL, IMUL. Pentium IMUL instructions. **(Quiz#5)**	Chapter7 (Assembly) & Advanced Arithmetic (Online)
35	M 10/12	**Division Instructions**: DIV, IDIV. Sign Extension Instructions: CBW, CWD, CDQ. Translating Arithmetic Expressions, Decimal string to number conversions. Number to decimal string conversion.	Chapter7 (Assembly) & Advanced Arithmetic (Online)
36	W 12/12	**String Instructions**: MOVS, MOVSB, MOVSW, MOVSD. REP Prefix.	String Handling Instructions (Online)
		HAJJ BREAK	
37	S 29/12	**String Instructions**: CMPS, CMPSB, CMPSW, CMPSD. SCAS, SCASB, SCASW, SCASD, LODS, LODSB, LODSW, LODSD, STOS, STOSB, STOSW, STOSD, REPE, REPNE. Applications of string instructions. **Input/Output**: IN and OUT instructions, Direct and Indirect I/O. **Introduction to Interrupts**. Difference between interrupts and procedures.	Chapter9 (Assembly) String Handling Instructions & Input/Output Instructions & Interrupts (Online)
38	M 31/12	Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag. Interrupt Processing, IVT, Trap Flag. **CPU Design**: Register Transfer.	Interrupts (Online)
	M 31/12	MAJOR EXAM II	
39	W 2/1	**CPU Design**: Register Transfer. **Data-Path Design**. Connecting Registers using Muxs. Connecting Registers using a tri-state bus. Examples of register transfer: MOV, XCHG, ADD.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
40	S 5/1	Examples of register transfer: SUB, INC, DEC. **Single-Bus CPU Data path design**:	Section 2.6 & Chapter 4

		Fetch Control Sequence. **(Solution of Major Exam II).**	(Organization) & CPU Design (Online)
41	M 7/1	**Single-Bus CPU**: Synchronous vs. Asynchronous Memory Transfer, Execution control sequence for ADD with register indirect addressing mode, unconditional & Conditional JMP, Add with immediate, CMP. **(Quiz#6)**	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
42	W 9/1 (Ext.)	**Single-Bus CPU**: Execution control sequence for Loop instruction. Performance Considerations. **Two-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump. **Three-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD, unconditional and conditional Jump Instructions.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
43	S 12/1	**Control Unit Design: Hardwired Control Unit,** General Hardwired Control Unit Organization, Generation of Control Signals. Deriving Rout & Rin Signals. **CPU-Memory Interface Circuit.**	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
44	M 14/1	**CPU-Memory Interface Circuit. Microprogrammed Control Unit Design*:*** Control Word, Control Store, Micro Program Counter, Micro Instruction Register, Microinstruction, Microroutine. General Organization of Micro-programmed Control Unit, Branching Address, Sequencer.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)
45	W 16/1	Horizontal, Field-encoded and vertical control store. Comparison of Hardwired vs. Micro-programmed control unit. Simple CPU Design Example.	Section 2.6 & Chapter 4 (Organization) & CPU Design (Online)