KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 061 Lecture Breakdown

	Date	Topics	Ref.
	S 9/9		
1	U 10/9	Syllabus. **Introduction**.	
2	T 12/9	Computer System, CPU, Memory, CPU-Memory Interface, Data Bus, Address Bus, Control Bus. Machine Type.	Chapter1 (Organization) & Introd. Computer Org. & Assembly Lang. Prog. (Online)
	S 16/9		
3	U 17/9	Memory Hierarchy: RAM, ROM. Cache, Registers. Machine Language, Assembly Language. Instruction Formats, Opcode, Operands. Stored Program Concept, **Fetch-Execute Cycle**, Instruction Pointer. Instruction Register.	Chapter1 (Organization) & Introd. Computer Org. & Assembly Lang. Prog. (Online) Section 2.1 (Assembly)
	M 18/9 (Makeup)	**Fetch-Execute Cycle**, Instruction Pointer. Instruction Register. **Why assembly language programming**. Data Typing in High Level and Assembly Language.	Chapter1 (Organization) & Introd. Computer Org. & Assembly Lang. Prog. (Online) Section 2.1 (Assembly)
4	T 19/9	No Class.	
	S 23/9		
5	U 24/9	Programmer's view of the computer, **Instruction Set Architecture** (ISA). ISA of i8086 processor. Interfacing the CPU to memory & I/O. **Number representation**: Binary, Octal, Hex. base conversion, fraction representation.	Introd. Computer Org. & Assembly Lang. Prog. (Online) Chapter 1 (Assembly)
6	T26/9	**Signed Number Representation**: Sign-magnitude, 1's complement, 2's complement. Sign Extension. Overflow detection for unsigned and signed numbers. **(Quiz#1)**	Introd. Computer Org. & Assembly Lang. Prog. (Online) Section 1.3

			(Assembly)
	S 30/9		
7	U 1/10	**Character Representation**. ASCII Code. Even and Odd Parity. Basic Elements of Assembly Language, **Assembly language syntax & Program Structure.**	Introd. Computer Org. & Assembly Lang. Prog. (Online) Section 1.3 (Assembly) Chapter 3 (Assembly)
8	T3/10	Flat Memory Program Template, Assembling, Linking, and Debugging Programs, **Variable Declaration**: DB, BYTE, SBYTE. Defining strings.	Variable, Constant, and Array Declaration (Online) Chapter 3 (Assembly)
	S 7/10		
9	U 8/10	DUP Operator, DW, WORD, SWORD, DD, DWORD, SDWORD, Byte Ordering, Defining Symbolic Constants, =, EQU, TEXTEQU. **(Quiz#2)**	Variable, Constant, and Array Declaration (Online) Chapter 3 (Assembly)
10	T 10/10 (Extend.)	Assembler Directives & Operators: Offset , Align, Type, Lengthof, sizeof, PTR, Label. IA32 Registers, Status & Flags Register, Memory Segmentation, Logical and Physical address translation.	Chapter 4 (Assembly) & Chapter 2 (Assembly)
	S 28/10		
11	U 29/10	**Basic Pentium Instructions**: MOV, XCHG. MOVZX, MOVSX, ADD, SUB.	Chapter 4 (Assembly) Basic Pentium Instructions (Online)
12	T 31/10	INC, DEC, NEG, ADC, SBB, JMP and LOOP Instructions. **Addressing Modes**: Immediate, Register, Direct, Register-Indirect.	Chapter 4 (Assembly) Unit4: Basic Pentium Instructions &Addressing Modes (Online)
	Th Nov. 2	**MAJOR EXAM I**	
	S 4/11		
13	U 5/11	Addressing modes: Based, Indexed, Based-Indexed. Solution of Major Exam I.	Chapter 4 (Assembly) &Addressing Modes (Online)
14	T 7/11	8086 Addressing modes. Link Library	Chapter5

		Overview, Calling a Library Procedure, Linking to a Library, Input/Output procedures using book's library (Irvine32.lib).	(Assembly)
	S 11/11		
15	U 12/11	Input/Output libraries, **Stack instructions**: Push and Pop.	Chapter5 (Assembly)
16	T 14/11	Stack instructions: PUSHAD, POPAD, PUSHFD, POPFD. **Introduction to procedures**. Defining and Using Procedures.	Chapter5 (Assembly)
	S 18/11		
17	U 19/11	**Logical Instructions**: NOT, AND, OR, XOR, Test, NOT. Applications of logic instructions.	Chapter6 (Assembly) & Bit Manipulation Instructions (Online)
18	T 21/11	No Class.	
	S 25/11		
	S 25/11 (Makeup)	**Flow Control Instructions**: CMP Instruction. Conditional Jump instructions: Signed and Unsigned. Single-flag jump instructions. Conditional Loop Instructions: Loope/Loopz, Loopne/Loopnz.	Chapter6 (Assembly) & Flow Control Instructions (Online)
19	U 26/11	High-Level Decision Control Structures: IF-Then-Else, For Loop, Case. While Loop, Repeat Until. Indirect Jump Example. **Shift Instructions**: SHL, SAL, SHR, SAR.	Chapter6 & 7 (Assembly) & Flow Control Instructions (Online)
20	T 28/11	**Shift Instructions**: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication. Applications of using shift instructions in performing division. SHLD, SHRD. **Rotate Instructions**: ROL, ROR, RCL, RCR. Applications of rotate instructions.	Chapter7 (Assembly) & Bit Manipulation Instructions (Online)
	S 2/12		
21	U 3/12	**Multiplication Instructions**: MUL, IMUL. Pentium IMUL instructions. **Division Instructions**: DIV, IDIV. Sign Extension Instructions: CBW, CWD, CDQ.	Chapter7 (Assembly) & Advanced Arithmetic (Online)
22	T 5/12	Translating Arithmetic Expressions, Decimal string to number conversions. Passing procedure parameters to the stack, RET N instruction, use of local variables.	Chapter7 (Assembly) & Advanced Arithmetic (Online)

	S9/12		
23	U10/12	**Input/Output**: IN and OUT instructions, Direct and Indirect I/O. **Introduction to Interrupts**. Difference between interrupts and procedures. Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag. Interrupt Processing, IVT, Trap Flag.	Input/Output Instructions & Interrupts (Online)
24	T 12/12	Bios and DOS interrupts. **String Instructions**: MOVS, MOVSB, MOVSW, MOVSD. REP Prefix. CMPS, CMPSB, CMPSW, CMPSD. SCAS, SCASB, SCASW, SCASD, LODS, LODSB, LODSW, LODSD, STOS, STOSB, STOSW, STOSD, REPE, REPNE. Applications of string instructions.	Interrupts & String Handling Instructions (Online)
	S 16/12		
25	U 17/12	**Major Exam II**.	
26	T 19/12	**CPU Design**: Register Transfer. **Data-Path Design**. Connecting Registers using Muxs. Connecting Registers using a tri-state bus. Examples of register transfer: MOV, XCHG.	Chapter 2 & 4 (Organization) & CPU Design (Online)
	S 6/1		
27	U 7/1	**Single-Bus CPU Data path design**: Fetch Control Sequence, Synchronous vs. Asynchronous Memory Transfer, Execution Control Sequence for MOV, XCHG, ADD.	Chapter 2 & 4 (Organization) & CPU Design (Online)
	M 8/1 (Makeup Class)	**Single-Bus CPU**: Execution control sequence for ADD with register indirect addressing mode, unconditional & Conditional JMP, INC, Loop, CMP, PUSH instructions. **Register Transfer Timing**: Estimating Minimum Clock Period. Performance Considerations. **Two-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump.	Chapter 2 & 4 (Organization) & CPU Design (Online)
28	T 9/1	**Three-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD, unconditional and conditional Jump Instructions. **Control Unit Design: Hardwired Control Unit**, General Hardwired Control Unit Organization, Generation of Control Signals. Deriving Rout & Rin Signals.	Chapter 2 & 4 (Organization) & CPU Design (Online)
	S 13/1		

29	U 14/1	**CPU-Memory Interface Circuit. Microprogrammed Control Unit Design*:*** Control Word, Control Store, Microinstruction, Microroutine.	Chapter 2 & 4 (Organization) & CPU Design (Online)
30	T 16/1	**Microprogrammed Control Unit Design*:*** Control Word, Control Store, Microinstruction, Microroutine. General Organization of Microprogrammed Control Unit, Micro Program Counter, Micro Instruction Register, Branching Address, Sequencer. Horizontal, Field-encoded and vertical control store. Comparison of Hardwired vs. Microprogrammed control unit.	Chapter 2 & 4 (Organization) & CPU Design (Online)