KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 052 Lecture Breakdown

Lec #	Date	Topics	Ref.	Lab
	S 10/9			Introduction, using MASM
1	M 13/2	Syllabus. **Introduction**. Computer System, CPU, Memory, CPU-Memory Interface, Data Bus, Address Bus, Control Bus. Machine Type. Memory Hierarchy: RAM, ROM.	Chapter1 (Organization) & Chapter 1 (Assembly)	
2	W 15/2	Cache, Registers. Machine Language, Assembly Language. Instruction Formats, Opcode, Operands. Stored Program Concept,	Chapter1 (Organization) & Chapter 1 (Assembly)	
3	Th 16/2	**Fetch-Execute Cycle**, Instruction Pointer. Instruction Register. **Why assembly language programming**. Data Typing in High Level and Assembly Language, Assembler, Linker, Debugger. Programmer's view of the computer, **Instruction Set Architecture** (ISA).	Chapter1 (Organization) & Chapter 1 (Assembly)	
	S 18/2			Introduction, using MASM
4	S 18/2	ISA of i8086 processor. Interfacing the CPU to memory & I/O. Types of Buses. One and Two-bus Architectures. **Number representation**.	Chapter1 (Organization) & Chapter 1 (Assembly) Appendix A & E (Assembly)	
5	M 20/2	**Number representation**: Binary, Octal, Hex. base conversion, fraction representation, unsigned and signed numbers **Signed Number Representation**: Sign-magnitude, 1's complement, 2's complement. Sign Extension. Overflow detection for unsigned and signed numbers.	Appendix A & E (Assembly)	
6	W 22/2	**Character Representation**. ASCII Code. Even and Odd Parity. **(Quiz#1)**	Appendix A & E (Assembly)	

	S 25/2			Assembly Format &Data Representation
7	S 25/2	**Assembly language syntax & Program Structure.** Instruction types. Assembler directives.	Chapter 3 (Assembly)	
8	M 27/2	**Variable Declaration**: DB, DW, DD. PTR operator. Offset operator. Constant declaration using EQU.	Chapter 3 (Assembly)	
9	W 1/3	DUP operator. Input/Output using INT 21H.: Reading character, Displaying character, Displaying a string. LOOP Instruction.	Chapter 3 & Section 12.5 (Assembly)	
	S 4/3			Input/Output
10	S 4/3	Input/Output using INT 21H.: Reading character, Displaying character, Displaying a string, Reading a string.	Chapter 3 & Section 12.5 (Assembly)	
	U 5/3	Replacing CR with '$' character **, 8086 registers**. **Memory Segmentation**, Logical & Physical Address.	Chapter 3 & 5 (Assembly)	
11	M 6/3	**(Quiz#2)**		
12	W 8/3	No class.		
	S 11/3			Segment. & Addressing Modes
13	S 11/3	**Memory Segmentation**, Logical & Physical Address. **8086 Addressing Modes**: Immediate, Register, Direct, Register-Indirect.	Chapter 3 & 5 (Assembly)	
14	M 13/3	**8086 Addressing Modes**: Based, Indexed, Based-Indexed.	Chapter 3 & 5 (Assembly)	
15	W 15/3	**Pentium Registers**. **Pentium Addressing Modes**. (Quiz#3).	Chapter 3 & 5 (Assembly)	
	S 18/3			Array indexing & Pentium Address. Modes
16	S 18/3	Status & Flags Register. **Basic Pentium Instructions**: MOV, XCHG.	Chapter 3 & 5 & 6 (Assembly)	
17	M 20/3	**Basic Pentium Instructions**: XCHG, LEA, MOVZX, MOVSX, XLATB, ADD, INC.	Chapter 3 & 5 & 6 (Assembly)	
18	W 22/3	**Basic Pentium Instructions**: SUB, DEC, NEG. CMP instruction, Introduction to flow control instructions.	Chapter 3 & 5 & 6 (Assembly)	

	S 25/3			Arithmetic Instructions
19	S 25/3	ADC, SBB. Review for Exam I.	Chapter 3 & 5 & 6 (Assembly)	
	U 26/3	**MAJOR EXAM I**		
20	M 27/3	**Multiplication Instructions**: MUL, IMUL. Pentium IMUL instructions. **Division Instructions**: DIV, IDIV. Sign Extension Instructions: CBW, CWD, CDQ.	Chapter 3 & 5 & 6 (Assembly)	
21	W 29/3	Applications of Multiplication & Division instruction. Logical Instructions: NOT, AND, OR, XOR, Test. Applications of logic instructions.	Chapter 3 & 6 & 8 (Assembly)	
	S 1/4			Logical & Bitwise Instructions
22	M 3/4	**Shift Instructions**: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication. Applications of using shift instructions in performing division.	Chapter 3 & 6 & 8 (Assembly)	
23	W 4/4	HLD, SHRD. **Rotate Instructions**: ROL, ROR, RCL, RCR. Applications of rotate instructions.	Chapter 3 & 6 & 8 (Assembly)	
	S 8/4			Flow Control Instructions
24	S 8/4	**Flow Control Instructions**: Unconditional JMP. Types of jump target: Short, Near, Far. **(Quiz#4).**	Chapter 7 & 4 (Assembly)	
25	M 10/4	Conditional Jump instructions: Signed and Unsigned. Single-flag jump instructions. Loop Instructions: Loop, Loope/Loopz, Loopne/Loopnz.	Chapter 7 & 4 (Assembly)	
26	W 12/4	High-Level Decision Control Structures: IF-Then-Else, For Loop, Case. While Loop, Repeat Until. Indirect Jump Example. **The Stack**: PUSH and POP instructions.	Chapter 7 & 4 (Assembly)	
	S 15/4			Procedures & Macros
27	S 15/4	Stack instructions: PUSHA, POPA, PUSHAD, POPAD, PUSHF, POPF, PUSHFD, POPFD. **Introduction to Procedures**: CALL and RET	Chapter 7 & 4&10 (Assembly)	
28	M 17/4	Procedure Definition, Near and Far Procedures, RET n instruction. Passing Parameters to Procedures.	Chapter 7 & 4&10 (Assembly)	

29	W 19/4	**Introduction to Macros**. Macro Definition & Expansion. Pseudo parameters in macros. Macros versus procedures.	Chapter 10 (Assembly)	
	S 22/4			String Instructions
30	S 22/4	Macro Library. Examples of Macros. REP macros. **(Quiz#5)**	Chapter 10 (Assembly)	
31	M 24/4	REP and IRP macros. Conditional assembly.	Chapter 10 (Assembly)	
32	W 26/4	**String Instructions**: MOVS, MOVSB, MOVSW, MOVSD. REP Prefix. CMPS, CMPSB, CMPSW, CMPSD.	Chapter 9 (Assembly)	
	S 29/4			Interrupts
33	S 29/4	SCAS, SCASB, SCASW, SCASD, LODS, LODSB, LODSW, LODSD, STOS, STOSB, STOSW, STOSD, REPE, REPNE. Applications of string instructions. **Input/Output**: IN and OUT instructions, Direct and Indirect I/O. String I/O instructions.	Chapter 9 & 12 (Assembly)	
34	M 1/5	**Introduction to Interrupts**. Difference between interrupts and procedures. Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag. **(Quiz#6)**	Chapter 12 (Assembly)	
35	W 3/5	Interrupt Processing, IVT, Trap Flag, Bios and DOS interrupts.	Chapter 12 (Assembly)	
	S 6/5			Video Memory
36	S 6/5	Register Transfer. **Data-Path Design**. Connecting Registers using Muxs. Connecting Registers using a tri-state bus.	Chapter 2 & 4 (Organization)	
37	M 8/5 (Ext.)	Examples of register transfer: MOV, XCHG, ADD. Register Transfer Timing: Estimating Minimum Clock Period.. **Single-Bus CPU Data path design**. Single-Bus CPU design: Fetch Control Sequence.	Chapter 2 & 4 (Organization)	
38	W 10/5	**Single-Bus CPU Data path design**. Single-Bus CPU design: Synchronous vs. Asynchronous Memory Transfer, Execution Control Sequence for MOV, XCHG, ADD, INC, ADD with register indirect addressing mode, unconditional Jump.	Chapter 2 & 4 (Organization)	
	Th 11/5	**MAJOR EXAM II**		
	S 13/5			Using the Mouse

39	S 13/5	**Single-Bus CPU**: Execution control sequence for Conditional JMP, Loop, CMP, PUSH instructions.		
40	M 15/5 (Ext.)	Performance Considerations. **Two-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump. **Three-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD, unconditional and conditional Jump Instructions. **Control Unit Design: Hardwired Control Unit**, General Hardwired Control Unit Organization, Generation of Control Signals.	Chapter 2 & 4 (Organization)	
41	W 17/5 (Ext.)	Deriving Rout & Rin Signals. **CPU-Memory Interface Circuit.**		
	S 20/5			Serial Port
42	S 20/5	**Microprogrammed Control Unit Design*:*** Control Word, Control Store, Microinstruction, Microroutine. General Organization of Microprogrammed Control Unit, Micro Program Counter, Micro Instruction Register, Branching Address, Sequencer.	Chapter 2 & 4 (Organization)	
42	M 22/5	No class.		
44	W 24/5	**No class.**		
	S 27/5			Project
45	S 27/5	Control Unit Design*:* Sequencer, Horizontal, Field-encoded and vertical control store. Microroutine for Add instruction with 8 addressing modes. Wide branch addressing and Multiway branching. Bit Oring. Comparison of Hardwired vs. Microprogrammed control unit.	Chapter 2 & 4 (Organization)	