KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 051 Lecture Breakdown

	Date	Topics	Ref.	Lab
	S 10/9			Introduction, using MASM
1	S 10/9	Syllabus. **Introduction**. Computer System, CPU, Memory, CPU-Memory Interface, Data Bus, Address Bus, Control Bus. Machine Type. Memory Hierarchy: RAM, ROM.	Chapter1 (Organization) & Chapter 1 (Assembly)	
2	M 12/9	Cache, Registers. Machine Language, Assembly Language. Instruction Formats, Opcode, Operands. Stored Program Concept, **Fetch-Execute Cycle**, Instruction Pointer. Instruction Register.	Chapter1 (Organization) & Chapter 1 (Assembly)	
3	W 14/9	Fetch-Execute Cycle. **Why assembly language programming**. Data Typing in High Level and Assembly Language, Assembler, Linker, Debugger. Programmer's view of the computer, **Instruction Set Architecture** (ISA). ISA of i8086 processor.	Chapter1 (Organization) & Chapter 1 (Assembly)	
	S 17/9			Introduction, using MASM
4	S 17/9	Interfacing the CPU to memory & I/O. Types of Buses. One and Two-bus Architectures. **Number representation**: Binary, Octal, Hex. base conversion, fraction representation, unsigned and signed numbers. Sign-magnitude.	Chapter1 (Organization) & Chapter 1 (Assembly) Appendix A & E (Assembly)	
5	M 19/9	**Signed Number Representation**: Sign-magnitude, 1's complement, 2's complement. Sign Extension.	Appendix A & E (Assembly)	
6	W 21/9	Overflow detection for unsigned and signed numbers. **Character Representation**. ASCII Code.	Appendix A & E (Assembly)	
	S 24/9			Assembly Format &Data Representation
7	M 26/9	Even and Odd Parity. **Assembly language syntax & Program Structure. (Quiz#1)**	Appendix A & E	

			& Chapter 3 (Assembly)	
8	W 28/9	**Variable Declaration**: DB, DW, DD. PTR operator.	Chapter 3 (Assembly)	
	S 1/10			Input/Output
9	S 1/10	Offset operator. Constant declaration using EQU. DUP operator. **Input/Output using INT 21H**. **(Quiz#2)**	Chapter 3 & Section 12.5 (Assembly)	
10	M 3/10	Input/Output using INT 21H.: Reading character, Displaying character, Displaying a string, Reading a string.	Chapter 3 & Section 12.5 (Assembly)	
11	W 5/10	Replacing CR with '$' character, **Loop Instruction, 8086 registers**. **Memory Segmentation**, Logical & Physical Address.	Chapter 3 & 5 (Assembly)	
	S 8/10			Segment. & Addressing Modes
12	S 8/10	**8086 Addressing Modes**: Immediate, Register, Direct, Register-Indirect. **(Quiz#3)**	Chapter 3 & 5 (Assembly)	
13	M 10/10	**8086 Addressing Modes**: Based, Indexed, Based-Indexed. Two-dimensional array indexing.	Chapter 3 & 5 (Assembly)	
14	W 12/10	**Pentium Registers**. **Pentium Addressing Modes**. Status & Flags Register.	Chapter 3 & 5 (Assembly)	
	S 15/10			Array indexing & Pentium Address. Modes
15	S 15/10	Status & Flags Register. **Basic Pentium Instructions**: MOV.	Chapter 3 & 5 & 6 (Assembly)	
16	M 17/10	**Basic Pentium Instructions**: XCHG, LEA, MOVZX, MOVSX, BSWAP, XLATB, ADD, SUB, INC, DEC, NEG.	Chapter 3 & 5 & 6 (Assembly)	
17	W 19/10	CMP instruction, Introduction to flow control instructions.	Chapter 3 & 5 & 6 (Assembly)	
	S 22/10			Arithmetic Instructions
18	S 22/10	No class.		
19	M 24/10	ADC, SBB instruction. **Multiplication Instructions**: MUL, IMUL. Pentium IMUL instructions. **Division Instructions**: DIV, IDIV.	Chapter 3 & 5 & 6 (Assembly)	
20	W 26/10	Sign Extension Instructions: CBW, CWD, CDQ. Applications of Multiplication &	Chapter 3 & 6 & 8	

		Division instruction. Logical Instructions: NOT, AND, OR, XOR, Test. Applications of logic instructions.	(Assembly)	
	S 12/11			Logical & Bitwise Instructions
21	S 12/11	**Shift Instructions**: SHL, SAL, SHR, SAR. Applications of using shift instructions in performing multiplication. Applications of using shift instructions in performing division. SHLD, SHRD. **Rotate Instructions**: ROL, ROR, RCL, RCR. Applications of rotate instructions.	Chapter 3 & 6 & 8 (Assembly)	
22	M 14/11	Review of Shift & Rotate instructions. **Flow Control Instructions**: Unconditional JMP. **(Quiz#4)**.	Chapter 7 & 4 (Assembly)	
23	W 16/11	**Flow Control Instructions**: Unconditional JMP. Types of jump target: Short, Near, Far. Conditional Jump instructions: Signed and Unsigned. Single-flag jump instructions. Loop Instructions: Loop, Loope/Loopz, Loopne/Loopnz.	Chapter 7 & 4 (Assembly)	
	S19/11			Flow Control Instructions
24	S 19/11	High-Level Decision Control Structures: IF-Then-Else, For Loop, Case. While Loop, Repeat Until. Indirect Jump Example. **The Stack**: PUSH and POP instructions, PUSHA, POPA, PUSHAD, POPAD, PUSHF, POPF, PUSHFD, POPFD.	Chapter 7 & 4 (Assembly)	
25	M 21/11	**Introduction to Procedures**: CALL and RET Procedure Definition, Near and Far Procedures, RET n instruction.	Chapter 7 & 4 (Assembly)	
26	W 23/11	Passing Parameters to Procedures. **Introduction to Macros**. Macro Definition & Expansion. Pseudo parameters in macros.	Chapter 7 & 4&10 (Assembly)	
	S 26/11			Procedures & Macros
27	S 26/11	Macros versus procedures. Macro Library. Examples of Macros. REP macros.	Chapter 10 (Assembly)	
28	M 28/11	REP and IRP macros. **(Quiz#5)**	Chapter 10 (Assembly)	
29	W 30/11	Conditional assembly. List Control Directives. **String Instructions**: MOVS, MOVSB.	Chapter 9&10 (Assembly)	
	S 3/12			String Instructions
30	S 3/12	No Class.		

31	M 5/12	**String Instructions**: MOVS, MOVSB, MOVSW, MOVSD. REP Prefix. CMPS, CMPSB, CMPSW, CMPSD.	Chapter 9 (Assembly)	
32	W 7/12	SCAS, SCASB, SCASW, SCASD, LODS, LODSB, LODSW, LODSD, STOS, STOSB, STOSW, STOSD, REPE, REPNE. Applications of string instructions. **Input/Output**: IN and OUT instructions, Direct and Indirect I/O.	Chapter 9 & 12 (Assembly)	
	S 10/12			Interrupts
33	S 10/12	String I/O instructions. **(Quiz#6)**	Chapter 12 (Assembly)	
34	M 12/12	**Introduction to Interrupts**. Difference between interrupts and procedures. Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag, IVT.	Chapter 12 (Assembly)	
35	W 1412	Interrupt Processing, Trap Flag, Bios and DOS interrupts.	Chapter 12 (Assembly)	
	S 17/12			Video Memory
36	S 17/12	Register Transfer. **Data-Path Design**. Connecting Registers using Muxs. Connecting Registers using a tri-state bus.	Chapter 2 & 4 (Organization)	
37	M 19/12	Connecting Registers using a tri-state bus. Examples of register transfer: MOV, XCHG, ADD. Register Transfer Timing: Estimating Minimum Clock Period.	Chapter 2 & 4 (Organization)	
38	W 21/12	**Single-Bus CPU Data path design**. Single-Bus CPU design: Fetch Control Sequence, Synchronous vs. Asynchronous Memory Transfer, Execution Control Sequence for MOV, ADD.	Chapter 2 & 4 (Organization)	
	S 24/12			Using the Mouse
39	S 24/12	Execution Control Sequence for ADD with register indirect addressing mode, unconditional Jump, conditional Jump, INC, ADD with immediate, LOOP.	Chapter 2 & 4 (Organization)	
40	M 26/12	**Single-Bus CPU**: Execution control sequence for Loop, CMP, PUSH instructions. Performance Considerations. **Two-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump.	Chapter 2 & 4 (Organization)	
41	W 28/12	**Three-Bus CPU**: Fetch Control Sequence, Execution Control Sequence for ADD,	Chapter 2 & 4 (Organization)	

		unconditional and conditional Jump Instructions. **Control Unit Design: Hardwired Control Unit**, General Hardwired Control Unit Organization, Generation of Control Signals.		
	S 31/12			Serial Port
42	S 31/12	Deriving Rout & Rin Signals. **CPU-Memory Interface Circuit.**	Chapter 4 (Organization)	
42	M 2/1	CPU-Memory Interface Circuit. **Microprogrammed Control Unit Design*:*** Control Word, Control Store, Microinstruction, Microroutine. General Organization of Microprogrammed Control Unit, Micro Program Counter, Micro Instruction Register, Branching Address.	Chapter 2 & 4 (Organization)	
44	W 4/1	Microprogrammed Control Unit Design*:* Sequencer, Horizontal, and Field-encoded control store.	Chapter 2 & 4 (Organization)	
	S 21/1			Project
45	S 21/1	Vertical control store. Microroutine for Add instruction with 8 addressing modes. Wide branch addressing and Multiway branching. Bit Oring. Comparison of Hardwired vs. Microprogrammed control unit.	Chapter 2 & 4 (Organization)	