KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 205 Computer Organization & Assembly Language
Term 042 Lecture Breakdown

	Date	Topics	Ref.	Lab
	S 12/2			Introduction, using MASM
1	U 13/2	Syllabus. Introduction. Computer System, CPU, Memory, CPU-Memory Interface, Data Bus, Address Bus, Control Bus. Machine type. Memory Hierarchy: Registers, Cache,	Chapter1 (Organization) & Chapter 1 (Assembly)	
2	T 15/2	Machine Language, Assembly Language. Why assembly language programming. Instruction Formats, Opcode, Operands. Stored Program Concept, Fetch-Execute Cycle, Instruction Pointer. Instruction Register.	Chapter1 (Organization) & Chapter 1 (Assembly)	
	S 19/2			Introduction, using MASM
3	U 20/2	Data Typing in High Level and Assembly Language, Assembler, Linker, Debugger. Programmer's view of the computer, Instruction Set Architecture (ISA). i8086 processor characteristics, Control Unit & Datapath. Interfacing the CPU to memory & I/O. Types of Buses. One and Two-bus Architectures.	Chapter1 (Organization) & Chapter 1 (Assembly)	
4	T 22/2	Number representation: Binary, Octal, Hex., base conversion, fraction representation, unsigned and signed numbers. Sign-magnitude, 1's complement, 2's complement **(Quiz#1).**	Appendix A & E (Assembly)	
	S 26/2			Assembly Format &Data Representation
5	U 27/2	2's complement Ranges. Overflow detection for unsigned and signed numbers. Character Representation. ASCII Code.	Appendix A & E (Assembly)	
6	T 1/3	Even and Odd Parity. Assembly language syntax & Program Structure. Variable Declaration: DB. Constant declaration using EQU. Input/Output using INT 21H. Reading	Chapter 3 & Section 12.5 & (Assembly)	

		character, displaying character.		
	S 5/3			Input/Output
7	U 6/3	Variable Declaration: DW, DD. Offset and PTR operators. Displaying a string. **(Quiz#2)**	Chapter 3 & Section 12.5 & (Assembly)	
8	T 8/3	Array declaration and referencing. DUP operator. Reading a string. Loop Instruction.	Chapter 3 & Section 12.5 & (Assembly)	
	S 12/3			Segment. & Addressing Modes
9	U 13/3	8086 registers. Memory Segmentation, Logical & Physical Address. Addressing Modes: Immediate, Register, Direct, Register-Indirect, Based, Indexed, Based-Indexed.	Chapter 3 & 5 (Assembly)	
10	T 15/3	IA32 Registers. Addressing Modes: Register-Indirect, Based, Indexed, Based-Indexed. Pentium Addressing Modes**. (Quiz#3)**	Chapter 3 & 5 (Assembly)	
	S 19/3			Array indexing & Pentium Address. Modes
11	U 20/3	Status & Flags Register. Basic Pentium Instructions: MOV, XCHG, LEA, MOVZX, MOVSX, BSWAP, XLATB.	Chapter 3 & 5 & 6 (Assembly)	
12	T 22/3	Basic Pentium Instructions: ADD, SUB, INC, DEC, NEG, CMP. Introduction to flow control instructions.	Chapter 3 & 5 & 6 (Assembly)	
	S 26/3			Arithmetic Instructions
13	U 27/3	Solution of Exam I.		
14	T 29/3	ADC, SBB. Multiplication Instructions: MUL, IMUL. Pentium IMUL instructions. Division Instructions: DIV, IDIV. Sign Extension Instructions: CBW, CWD, CDQ, CWDE.	Chapter 6 & 3 (Assembly)	
	S 2/4			Logical & Bitwise Instructions
15	U 3/4	Logical Instructions: NOT, AND, OR, XOR, Test. Applications of logic instructions. Shift Instructions: SHL, SAL, SHR, SAR.	Chapter 3 & 6 & 8 (Assembly)	
16	T 5/4	Applications of using shift instructions in performing multiplication. Applications of using shift instructions in performing division. SHLD, SHRD. Rotate Instructions: ROL, ROR, RCL, RCR. Applications of rotate	Chapter 3 & 6 & 8 (Assembly)	

		instructions. **(Quiz#4)**		
	S 16/4			Flow Control Instructions
17	U 17/4	Flow Control Instructions: Unconditional JMP. Types of jump target: Short, Near, Far. Conditional Jump instructions: Signed and Unsigned. Single-flag jump instructions. Loop Instructions: Loop, Loope/Loopz, Loopne/Loopnz.	Chapter 7 & 4 (Assembly)	
18	T 19/4	Loop Instructions: Loop, Loope/Loopz, Loopne/Loopnz. High-Level Decision Control Structures: IF-Then-Else, For Loop, While Loop, Case, Repeat Until. Indirect Jump Example. The Stack: PUSH and POP instructions.	Chapter 7 & 4 (Assembly)	
	S 23/4			Procedures & Macros
19	U 24/4	Stack instructions: PUSHA, POPA, PUSHAD, POPAD, PUSHF, POPF, PUSHFD, POPFD. Introduction to Procedures: CALL and RET. **(Quiz#5)**	Chapter 7 & 4 (Assembly)	
20	T 26/4	Procedure Definition, Near and Far Procedures, RET n instruction. Passing Parameters to Procedures. Examples of Procedures.	Chapter 7 & 4 (Assembly)	
	S 30/4			String Instructions
21	U 1/5	Introduction to Macros. Macro Definition & Expansion. Pseudo parameters in macros. Macros versus procedures. Macro Library. Examples of Macros.	Chapter 10 (Assembly)	
22	T 3/5	String Instructions: MOVS, MOVSB, MOVSW, MOVSD. REP Prefix. CMPS, CMPSB, CMPSW, CMPSD, SCAS, SCASB, SCASW, SCASD, LODS, LODSB, LODSW, LODSD, STOS, STOSB, STOSW, STOSD, REPE, REPNE. Applications of string instructions.	Chapter 9 (Assembly)	
	S 7/5			Interrupts
23	U 8/5	Input/Output: IN and OUT instructions, Direct and Indirect I/O. Introduction to Interrupts. Difference between interrupts and procedures. **(Quiz#6)**	Chapter 12 (Assembly)	
24	T 10/5	Types of Interrupts: Hardware. Software, Exceptions. Maskable and non-maskable Interrupts, Interrupt Flag, IVT, Interrupt Mechanism, Bios and DOS interrupts.	Chapter 12 (Assembly)	

	S 14/5			Video Memory
25	U 15/5	CPU Design: Control unit and Data Path. Register Transfer. Data-Path Design. Connecting Registers using Muxs. Connecting Registers using a tri-state bus. Examples of register transfer: MOV, XCHG.	Chapter 2 & 4 (Organization)	
26	T 17/5	Register Transfer Timing: Estimating Minimum Clock Period. Single-Bus CPU Data path design. Single-Bus CPU design: Fetch Control Sequence, Synchronous vs. Asynchronous Memory Transfer, Execution Control Sequence for MOV, ADD, XCHG.	Chapter 2 & 4 (Organization)	
	S 21/5			Using the Mouse
27	U 22/5	Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump, INC, CMP, and LOOP. Performance Considerations. Two-Bus CPU: Fetch Control Sequence, Execution Control Sequence for ADD with register indirect addressing mode, unconditional and conditional Jump.	Chapter 2 & 4 (Organization)	
28	T 24/5	Three-Bus CPU: Fetch Control Sequence, Execution Control Sequence for, ADD, unconditional and conditional Jump Instructions. Control Unit Design: Hardwired Control Unit, General Hardwired Control Unit Organization, Generation of Control Signals. Deriving Rout & Rin Signals.	Chapter 4 (Organization)	
	S 28/5			Serial Port
29	U 29/5	CPU-Memory Interface Circuit. ***Microprogrammed Control Unit Design:*** Control Word, Control Store, Microinstruction, Microroutine. General Organization of Microprogrammed Control Unit, Micro- Program Counter, Micro Instruction Register.	Chapter 4 (Organization)	
30	T 31/5 (Extend.)	Sequencer, Branching Address. Horizontal, Vertical and Field-encoded control store. Microroutine for Add instruction with 8 addressing modes. Wide branch addressing and Multiway branching. Bit Oring. Comparison of Hardwired vs. Microprogrammed control unit.	Chapter 2 & 4 (Organization	