KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 203 Digital Design Lab

**Term 082 Lab Breakdown**

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| **Week#** | **Date** | **Topics** |
| 1 | S 28/2 | Syllabus. Introduction. Review of Combinational Circuit Design: K-Map, two-level logic minimization, prime and essential prime implicants, don't care conditions, multiplexers, decoders, implementing functions using multiplexers and decoders, modular design, adder/subtractor design. |
| 2 | S 7/3 | Review of Sequential Circuit Design: Latch vs. Flip Flop, analysis of sequential circuits, design of sequential circuits, counters design. Introduction to the prototyping board and use it to test a 74xx chip (OR). |
| 3 | S 14/3 | **Experiment#1**: Prototyping of Logic Circuits using Discrete Components. Implementation of a Full Adder using chips 7408 AND, 7432 (OR) and 7486 (XOR). |
| 4 | S 21/3 | **Experiment#2**: Implementation of sequence detector using EEPROM and D-FFs (7474). |
| 5 | S 28/3 | **Experiment#3**: Introduction to FPGA Design Flow. Implementation of a full-adder using FPGA. |
| 6 | S 4/4 | **Experiment#4:** Traffic Light Controller using FPGA. |
| 7 | S 11/4 | **Experiment#5:** |
|  | U 12/4 | Last Day for Dropping with W |
| 8 | S 18/4 | **Experiment#6:** always block, if & case statements. ALU modeling. |
|  | Apr. 25-30 | Midterm Vacation |
| 9 | S 2/5 | **Experiment#7:** FSM modeling in verilog, modeling and implementation of traffic light controller in verilog. |
| 10 | S 9/5 |  |
|  | U 10/5 | Last Day for Dropping all Courses with W |
| 11 | S 16/5 |  |
| 12 | S 23/5 |  |
| 13 | S 30/5 |  |
| 14 | S 6/6 |  |
| 15 | S 13/6 |  |