KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

COMPUTER ENGINEERING DEPARTMENT

COE 203 Digital Logic Laboratory
Syllabus - Term 082

Catalog Description

Review of Digital Logic Design: Design of Combinational Circuits, and Design of Sequential Circuits. Logic implementation using discrete logic components (TTL, CMOS), and programmable logic devices. Introduction to Field Programmable Logic Arrays (FPGAs). The basic design flow: design capture (schematic capture, HDL design entry, design verification and test, implementation (including some of its practical aspects), and debugging. Design of data path and control unit.
Prerequisite: COE 202

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Office Hours SMW 11:00-12:00**,** and by appointment

Course Objectives

After successfully completing the course, students will be able to:

1. Design combinational and sequential circuits using discrete components, EEPROMs, and FPGAs to meet certain specifications.
2. Use basic structural Hardware Description Languages to implement digital circuits.
3. Design and conduct experiments related to digital systems and to analyze their outcomes.

Course Learning Outcomes

1. Ability to design combinational and sequential circuits to meet certain specifications.
2. Ability to use tools and discrete components, EEPROMs, FPGAs, to model, simulate and implement digital circuits
3. Ability to design and conduct experiments related to digital systems and to analyze their outcomes.
4. Ability to work in teams.
5. Ability to communicate effectively.

Text Book

Morris Mano and Charles Kime, Logic and Computer Design Fundamentals, Third Edition, Prentice Hall International, 2004

Grading Policy

Discussions & Reflections	5%
Lab Work	75%
Project	20%

Course Topics

1. ***Combinational Logic Design Review.*** **1 week**
   - K-maps and logic minimization
   - XORs, XNORs, Decodes, MUXs, Adders, Subtractors

2. ***Sequential Logic Design Review.*** **1 week**
   - Flip-flops
   - Sequential circuits design procedure
   - Sequential circuits analysis procedure
   - Counters and Registers

3. ***Prototyping of logic circuits.***

   i. Discrete components **(Experiment 1)** **1 week**
   - Introduction to ICs, logic families, 74xx and 54xx
   - Power and ground
   - Physical implementation of combinational circuits using discrete components
   - Implementation of a simple combinational circuit using ICs.

   ii. EEPROM **(Experiment 2)** **1 week**
   - Introduction to logic prototyping using PLDs.
   - Implementation of a sequential circuit using EEPROMs and external registers.

   iii. FPGAs
   - Introduction to FPGAs design flow **(Experiment 3)** **1 week**
   - Design and implementation of a sequential circuit using schematic design entry. **(Experiment 4)** **1 week**
   - Introduction to hardware description languages (HDL)
     - Structural modeling using verilog
     - Complete design and implementation of a small combinational circuit **(Experiment 5)** **1 week**
   - Register Transfer Level (RTL) modeling using verilog
     - Complete design and implementation of a simple datapath **(Experiment 6)** **1 week**
   - Sequential circuit implementation using verilog **(Experiment 7)** **1 week**

4. ***Design and implementation of a data path and control unit.***
   - Integrating HDL and schematic units

   (Experiment 8) **2 weeks**

5. ***Project.*** **3 weeks**