Ref: Online course on EE-390, KFUPM

Handout 19

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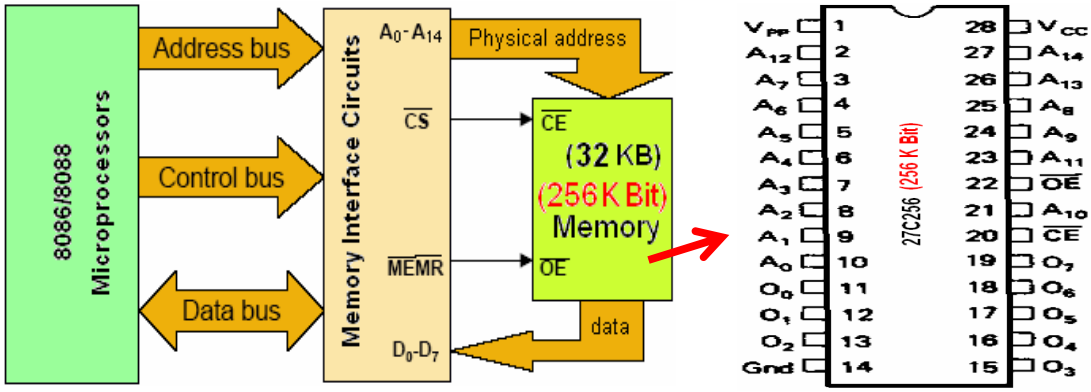
Properties and Organization of Memory Subsystems

Objective:

- To discuss basic properties of memory system.
- To analyze the organization and expansion techniques of memory system.

Slide 1: **<u>Accessing Read Only Memories</u>:**

- Block diagram and pin layout of a 256 KB EPROM is shown:



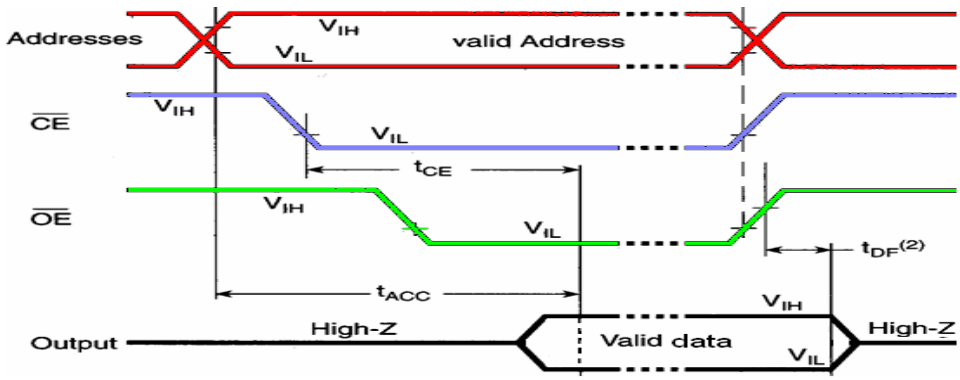
- The read cycle includes: (1) Applying valid physical address, (2) Apply proper control signals and (3) Read the stored data. The memory interface circuit is described in lecture 3 of this module.

<u>Note: The pin configuration of the EPROM is also shown here. Note that the capacity of this EPROM is 32 KB.</u>

<u>Similar accessing method is also used for other type of primary memories.</u>

Slide 2: **Accessing EPROM (cont'd):**

- The programming algorithm of Intel 27C256 EPROM is shown:



Note: ***Extra speech: some of the important parameters of this read bus cycle are:***

- Access-time (t_{ACC}), is the address-to-output delay (170 - 250ns) Often wait-status is inserted to interface with faster CPU.

- Chip-enable-time (t_{CE}), represents chip-enable-to-output delay. This time delay provides stable data-output after $\overline{CE}$➔'0'.

- Chip-deselect-time (t_{DF}) represents recovery time for the output and the time delay introduced by the ROM chip.

Slide 3: **Poplar EPROM IC's:**

- *Click here for tabulated capacity of popular EPROM IC's.*

Hyperlinked Table

EPROM	Density (bits)	Capacity (bytes)
2716	16K	2K x 8
2732	23K	4K x 8
27C64	64K	8K x 8
27C128	128K	16K x 8
27C256	256K	32K x 8
27C512	512K	64K x 8
27C010	1M	128K x 8
27C020	2M	256K x 8
27C040	4M	512K x 8

Note: ***The pin layout and access bus cycle of the intel 27C256 are presented previously.***

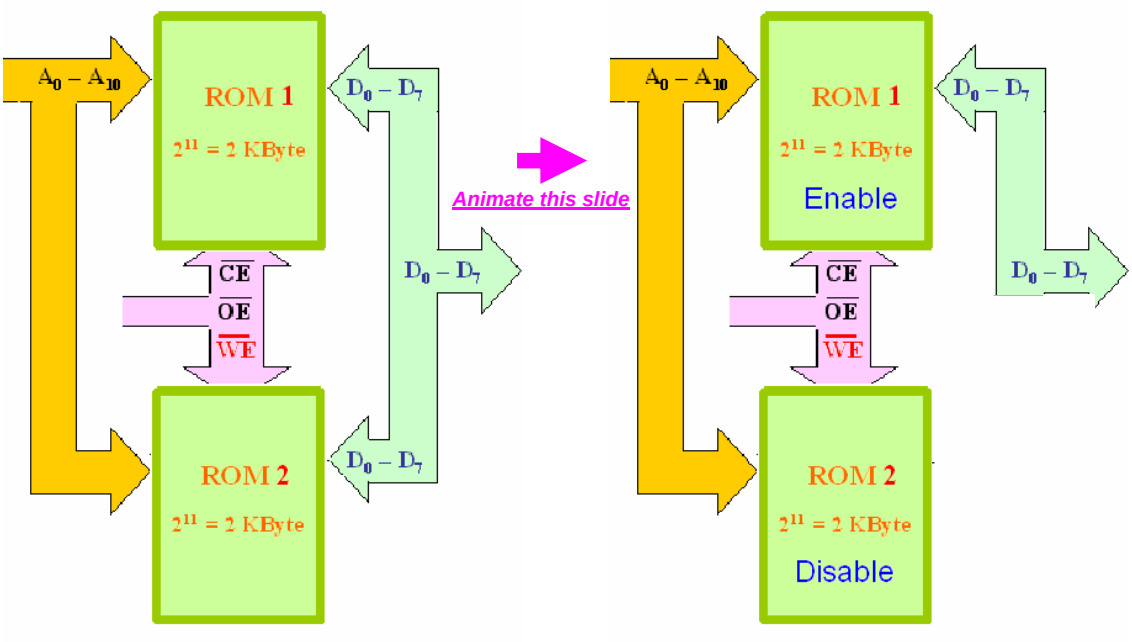
- The timing characteristics of Intel 27C256 EPROM are:
  - t_{ACC} (Address to output delay) = 250 ns maximum
  - t_{CE} (CE to output delay) = 250 ns maximum
  - t_{OE} (OE to output delay) = 100 ns maximum
  - t_{DF} (OE high to output high-Z) = 60 ns maximum
  - V_{IH} (Minimum input voltage to be recognized as 'logic 1') = 2.4 V
  - V_{IL} (Maximum input voltage to be recognized as 'logic 0') = 0.45 V
  - V_{OH} (Minimum output voltage to be recognized as 'logic 1') = 2.0 V
  - V_{OL} (Maximum output voltage to be recognized as 'logic 0') = 0.8 V

Note: ***These constitute important characteristics for temporary memory devices.***

Slide 4: **Expanding the Storage Capacity of EPROM:**

- Often application requires more storage locations then what is provided by any single memory (EPROM) IC.

- One popular way to expand the capacity is to integrating more ROM chips to increase the total memory storage. Such as,



Note:: ***Let's assume two ROM IC's are connected as shown above. Note that at any given moment; only one ROM can be activated and accessed by data bus. Thus, two ROM chips are integrated here to increase the storage capacity or word capacity of the stored data.***

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Slide 5: **Expanding the Storage Length of EPROM (cont'd):**

- Another popular way to expand the memory storage is by increasing the storage length. This integrates two or more ROM's in a manner, shown below, and used in 8086 systems

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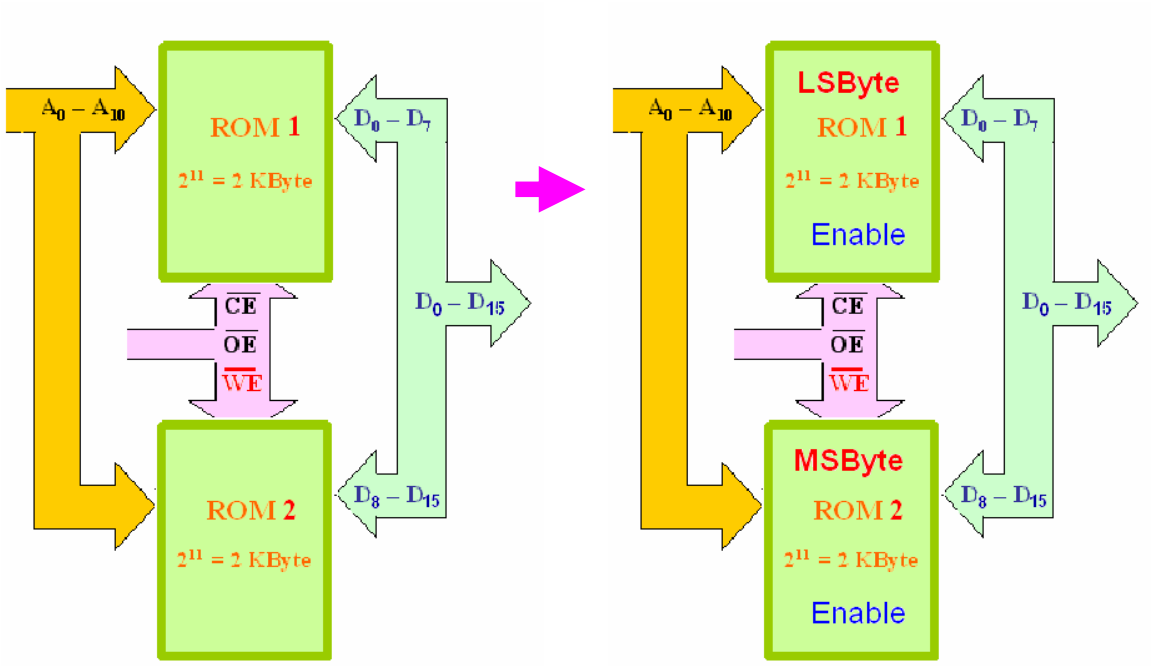
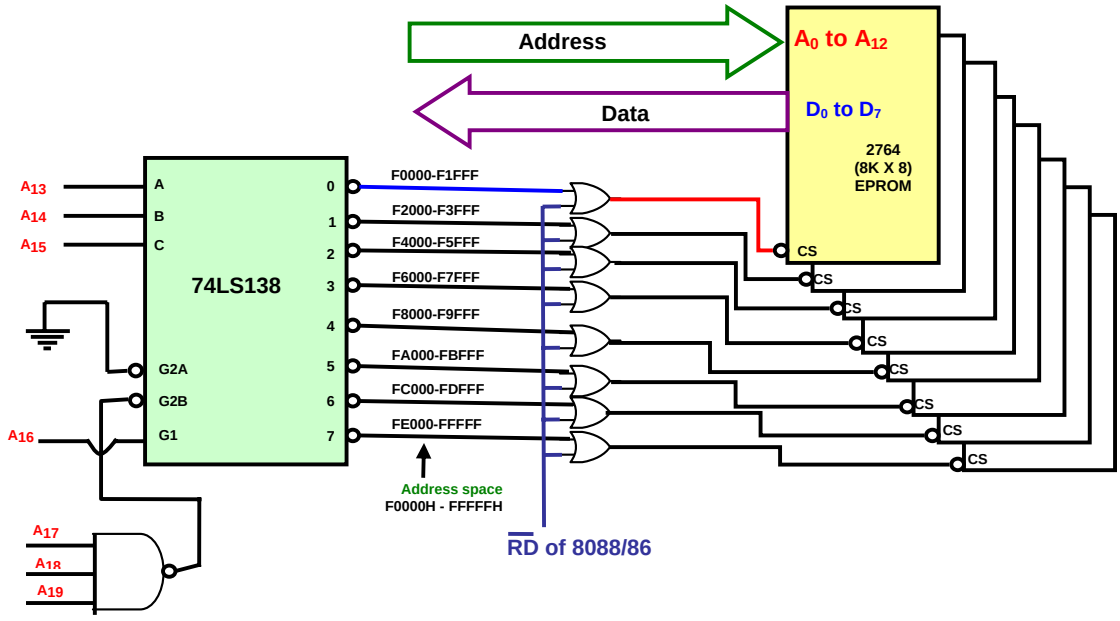


Note: ***In this method, expanding word or storage length, means expanding each memory location from 8-bit configuration to 16-bit configuration. This is particularly useful for 8086 systems with 16-bit data bus***

Slide6: **Memory Address Decoding:**

- The decoding process used to access 64 KB of data, stored in eight EPROM IC's (8KB-capacity per IC), are shown below.

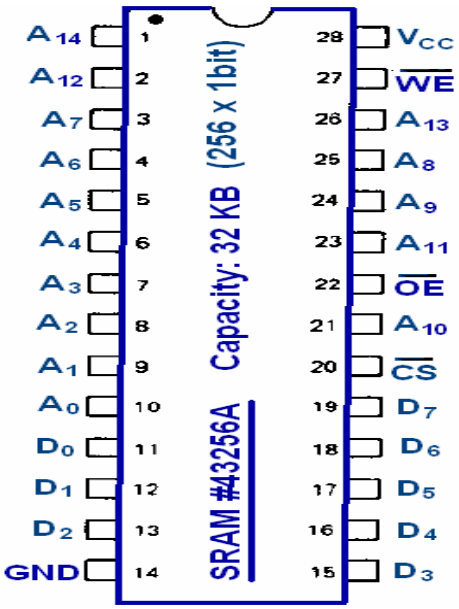


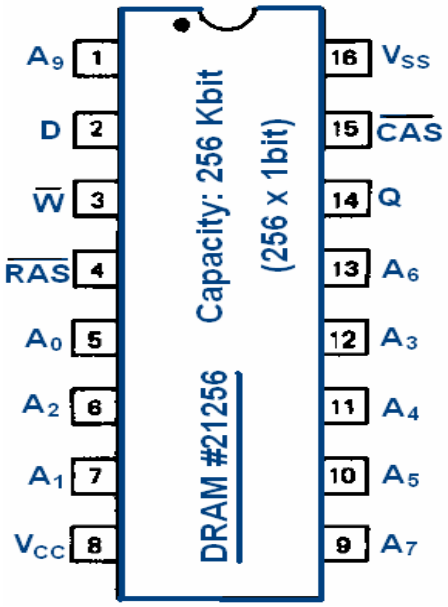
Note: ***Note that Address pins A13 to A15 are used to select the EPROM IC's by providing the decided signal in its chip select input.***

The Address pins A16 to A19 are used to enable the decoder. Since each 2764 EPROM's have storage capacity of 8 kilo Byte (with physical address of 0000 to 1FFF Hex), and the decoder can select 8 EPROM's, the total memory location that can be accessed by this circuit is 64 kilo Byte.

Slide7: **Popular SRAM and DRAM IC's:**

- DRAM storage is more compact due to its array like storage. Both memory IC's with a density of 256 Kbits are shown below:





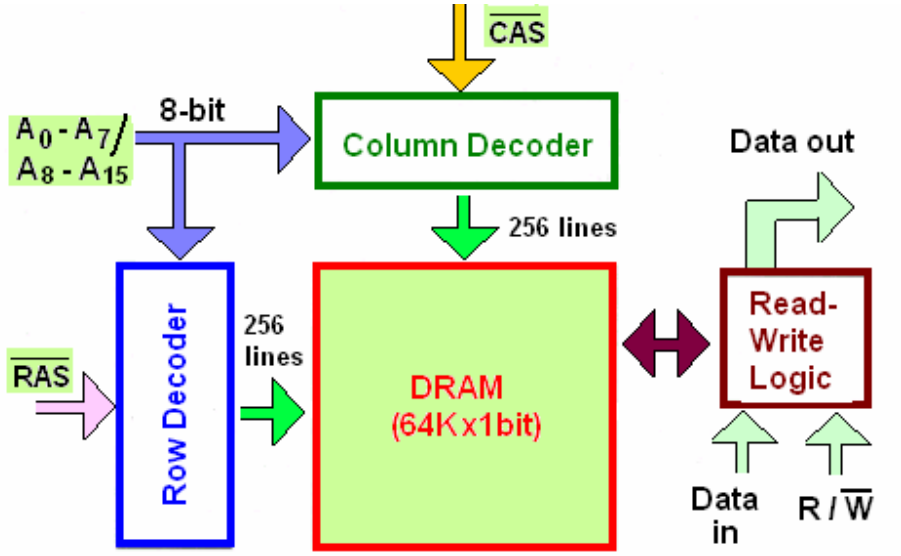
- *Click here for tabulated capacity of popular RAM IC's.*

Hyperlinked Table

SRAM	Density (bits)	Capacity (bytes)
4361	64K	64K x 1
4364	64K	8K x 8
43256A	256K	32K x 8
431000A	1M	128K x 8
DRAM	**Density (bits)**	**Capacity (bytes)**
21256	256K	256K x 1
424256	1M	256K x 4
416160	16M	1M x 16

Slide8: **Accessing SRAM and DRAM IC's:**

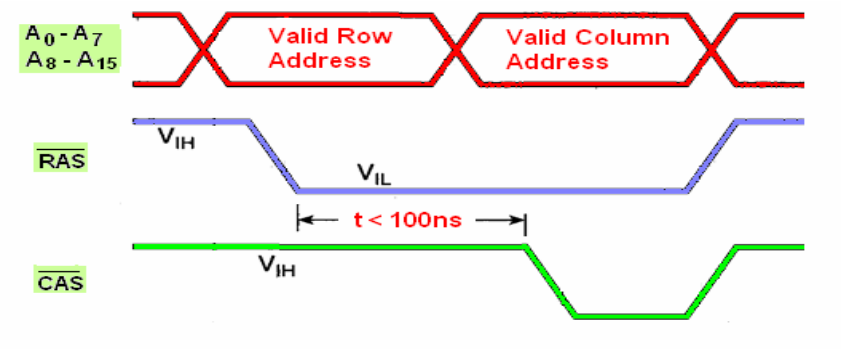
- SRAM is accessed in a similar manner as described in slide 2, but as DRAM storage locations are organized in an array, and uses time-multiplexed address pins with $\overline{CAS}$ and $\overline{RAS}$ signals.



Note: ***Thus, initially 8-bit row address is applied and RAS bar is pulsed to logic 0, to latch row address into the device.***
Next the column address is applied and strobes CAS bar to logic 0.
Thus, 16-bit address, applied using 8-bit bus using time multiplexing, is used to select one of the 64K storage locations.
The read write logic circuit is used to control the dara in and out process.

Slide9: **Accessing DRAM IC's (cont'd):**

- The access cycle of DRAM memory is shown below:



- In "page mode", even after row address is latched inside the DRAM, $\overline{RAS}$='0' is maintained to keep the row address valid.

- Then, by simply supplying multiple column address, multiple storage locations along the selected row can be accessed.

Note: ***This provides faster access of DRAM memory by eliminating the time needed to setup and strobe duplicated row addresses.***

To improve the reliability of information transfer, a parity bit is often added to each data-byte to implement a parity error checking mechanism.

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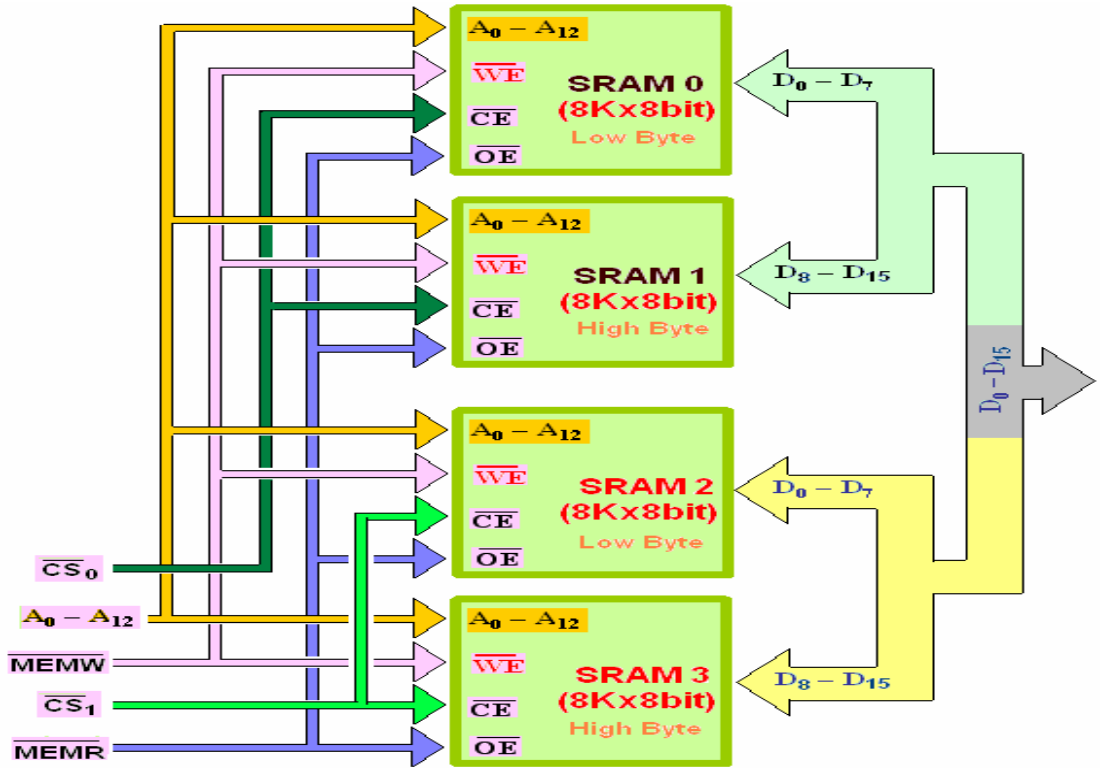
Slide10: **Designing Memory Systems:**

- Often memory IC's are inter-connected to form memory system. Such a 16Kx16bit memory system, using four 8Kx8bit SRAM's are:



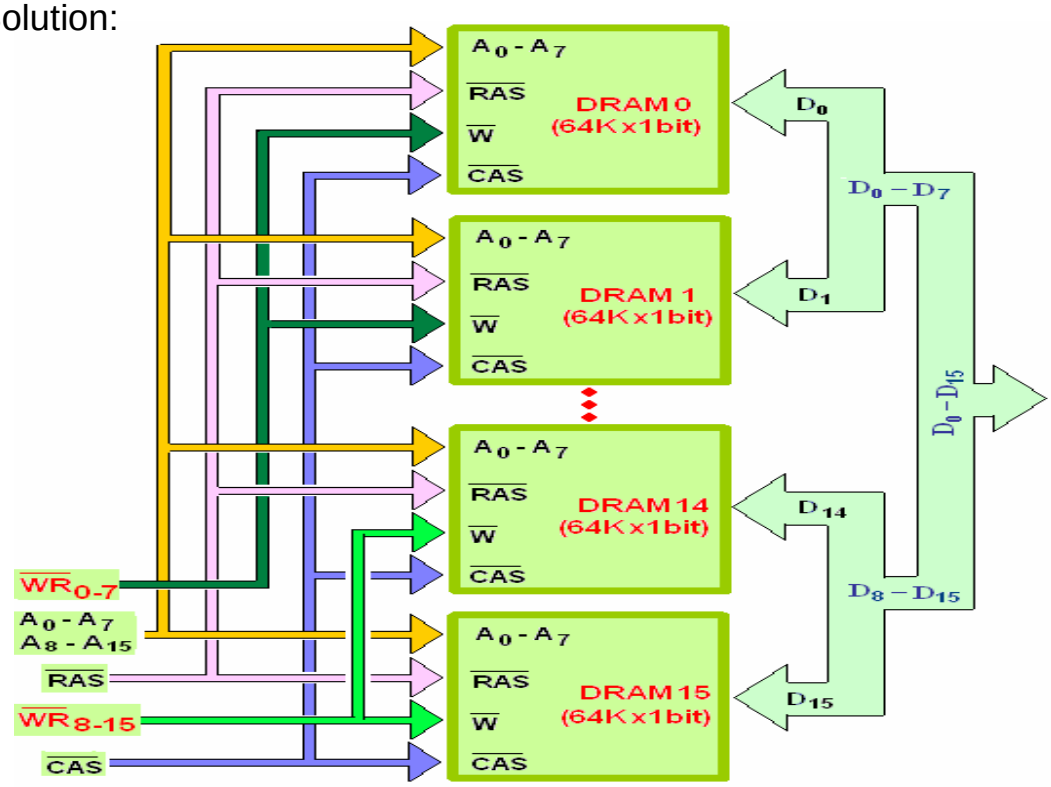
Note: ***Note this memory system only activates either SRAM0 & 1 or SRAM2 & 3, using the chip select CS0 or CS1. Once selected, these chips provide an access to total 8K, 16-bit wide storage locations.***

The Memory read and write control signals are provided by MEMR bar and MEMW bar and are inputted in the output enable (OE bar) and write enable (WE bar) pins of the SRAM chip.

Slide 11: **Example 1:**

Question: Design a memory system using sixteen 2164B DRAM IC's (organized in 64Kx1bit), to implement 64Kx16-bit storage.

Solution:



Note: ***Note that each DRAM IC stores 1 byte per memory location and has 64K storage locations. Thus, cascading 16 such DRAM IC's will allow us to organize the required 64Kx16bit storage.***

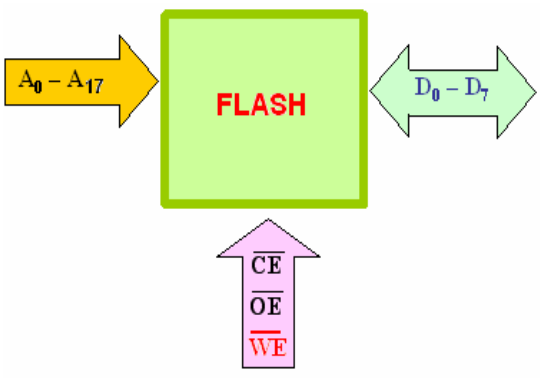
This DRAM IC can access 64K memory locations using only 2^8 address pins, due to the array like arrangement, which is controlled by column and row address strobe (CAS bar and RAS bar) signals.

Remember there are two write (WR bar) signals, where WR 0-7 bar accesses the 1st eight DRAM IC's, numbering from 0 to 7, and WR 8 – 15 bar accesses the last eight DRAM IC's, numbering from 8 to 15.
Logic low input for WR bar signal is initiates a write cycle and logic high input for WR bar signal initiates a read cycle.

Slide 12: **FLASH Memories:**

- The block diagram of FLASH memory is similar to EPROM with the exceptions of bidirectional data bus and Write enable pin

- This non-volatile read/write memory is erased and reprogrammed electrically



Note: ***Thus, FLASH uses EPROM like algorithm, although it is programmed and erased like EEPROM.***

- Standard FLASH memory array architectures are;
  (1) Bulk-erase,
  (2) Boot-block and
  (3) Flash-file

Note: ***The storage array in the bulk-erase device is a single block, whereas the memory arrays in the both the boot-block and Flash-File are organized as multiple independently erasable blocks.***

- The recent USB FLASH drives use FlashFile architecture, intended for large storage and is implemented as mass solid-state storage device. These memories support clock locking.

Slide 13: Example 2:

Question: Define Memory Capacity and Memory Organization.

Solution: Memory Capacity is the number of bits that a semiconductor memory chip can store and is called its chip capacity (bits or bytes)

Memory Organization: If each memory chip contains "2^n" storage locations, where 'n' is the number of address pins on the chip and each location is capable of storing "y" bits, where 'y' is the number of data pins on the chip, then the entire chip is said to be organized as (2^n)x(y bits). Such as, organization of a memory IC with 12 address pins and 4 data pins are: 2^{12} x 4 bits. This means that this memory IC has 2^{12} = 4096=4K locations, each holding 4 bits. Thus, organization of 4Kx4bit.

Slide 14: Example 3:

Question: In the memory system designed in Slide 10, the storage locations are expanded using:

(1) Storage capacity,
(2) Storage length,
(3) Both of above
(4) None of Above.

Solution: (3) both expansion methods (storage capacity and storage length) are used here to increase the memory size.

Slide 15: Exercise 1:

Question: Design a memory system for 8086 microprocessors using #416400 DRAM IC's (organized in 4Mx4bit), to implement "4M x 16-bit" storage.

Solution: The designed memory system is shown below: