Ref: Online course on EE-390, KFUPM

Handout 18

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Temporary storage Memories

Objective:

- To discuss different types of Temporary storage memory's (RAM and Cache) and FLASH memory

- To learn the operation and electronic circuits associated with these memory devices.

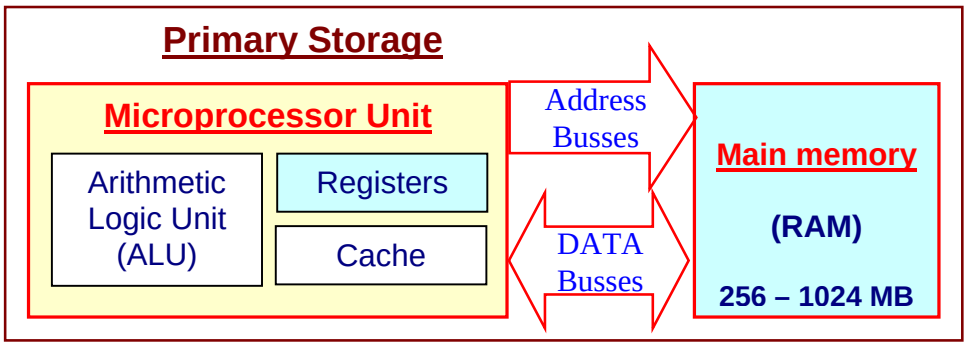
Slide 1: **Random Access Memory (RAM) or Main-memory:**

- RAM is volatile memory and stores programs that are currently being run by CPU and data these programs are operating on.

Note: volatile means information is stored as long as the power supply of the memory chip remains ON.

Recently, carbon nano-tubes and magnetic tunneling effects are investigated to develop non-volatile RAM's

- It is directly connected to CPU via high speed address and data busses for very quick information transfer between CPU registers and the storage locations of main memory (RAM).



- The word "random" means that any piece of stored data can be returned within a constant time, regardless of its location

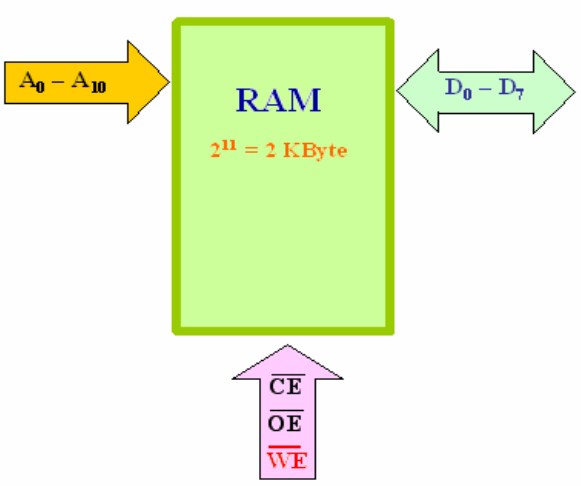
Slide 2: **Random Access Memory (Cont'd):**

- System RAM speed is controlled by bus-width and bus-speed

- Bus-width refers to the number of bits that can be sent to the CPU simultaneously, and bus-speed refers to the number of times a group of bits can be sent per second.

- The block diagram of a 2 K-Byte RAM is shown. Its memory interface circuits are discussed in previous module.

- The bi-directional data bus and the write enable signal introduce the writing capability of RAM.



Note:

- Note that unlike ROM, RAM has bi-directional Data Bus (**blink** $D_0 - D_7$) used for either reading or writing information.

- The width of the Address Bus (**blink** $A_0 - A_{10}$) determines the capacity of the storage. Here 11-bit address bus can access 2^{11}=2048 or 2 Kilo-Byte memory locations.

- The additional control signal, WE bar (**blink this in figure**) is used to enable writing process. Other control signals, CE bar and OE bar (**blink this in figure**) behaves in same way as ROM, and enables the desired RAM chip and its output circuitry, respectively.

Slide 3: **Commonly available RAM's:**

- Static random access memory (SRAM) retains its contents as long as supply power remains ON. Typically, they are used in low power and high speed circuits, like CPU cache, HD buffer ..

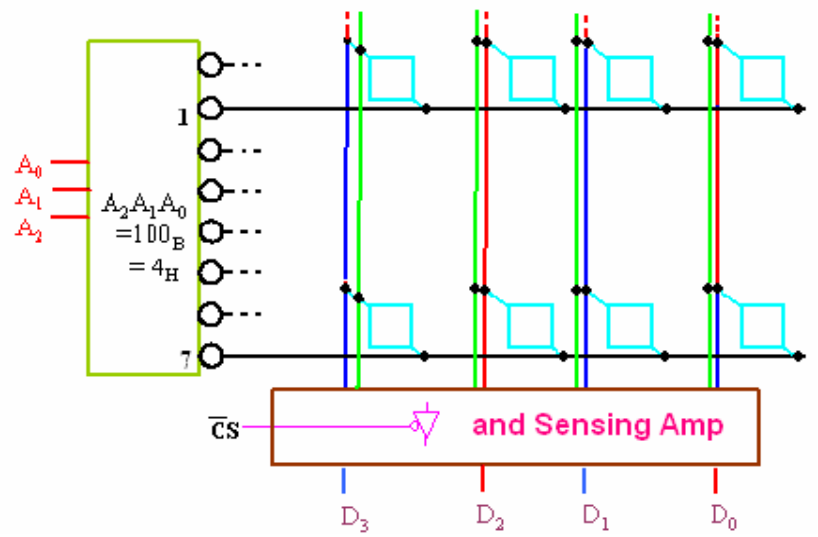
- Dynamic random access memory (DRAM) requires continues power supply and periodic refreshment to retain its contents. They are considerable small in size but power hungry.

- Evolution of Popular DRAM: Extended-Data-Out (EDO) DRAM, Synchronous (S) DRAM, Double data rate synchronous (DDRS) DRAM etc…

- For more information:http://en.wikipedia.org/wiki/Random_access_memory

Slide 4: **Electronics related to Static Read Only Memory (SRAM):**

- SRAM Storage cells, shown as blue boxes, typically consist of multiple (four to six) MOS transistors. The address decoder (with A_0-A_2) and output control circuit (with $\overline{CS}$) are also show.



- The address decoder outputs 'logic 0' level via selected or decoded output pin, which in return sends 'logic 0' output via D_1 to D_3 depending on the status of the storage cells (if ON).

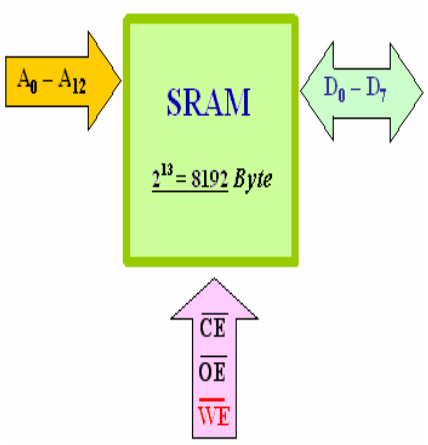
- The operating detail of this circuit is presented in next slide.

Slide 5: **Accessing SRAM Memory Storage Locations:**

- As this SRAM has 8-bit data bus, each of its storage is byte-wide.

- Thus, 13-bit physical address can access 2^{13} = 8192 byte one dimensional storage locations.

- For read/store bus cycle, set $\overline{WE}$='1' and for write/retrieve, $\overline{WE}$='0'

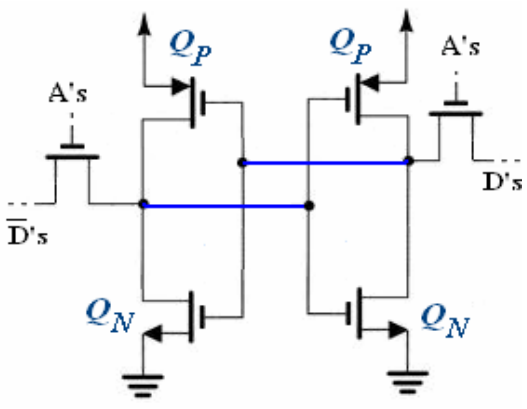


- Thus to access data from SRAM, we need to;
  (1) Apply **physical address**,
  (2) Apply control signals **$\overline{CE}$, $\overline{OE}$** and **$\overline{WE}$**

Note: Note that the control signals are important as they control important characteristics of RAM like Access time, Chip-enable time and Chip deselect time etc… These parameter will explained in next lecture.

Slide 6: **Electronics related to SRAM (Cont'd):**

- In each storage cell, the MOS transistors (Q_p's and Q_n's) constitute a cross-coupled inverter.

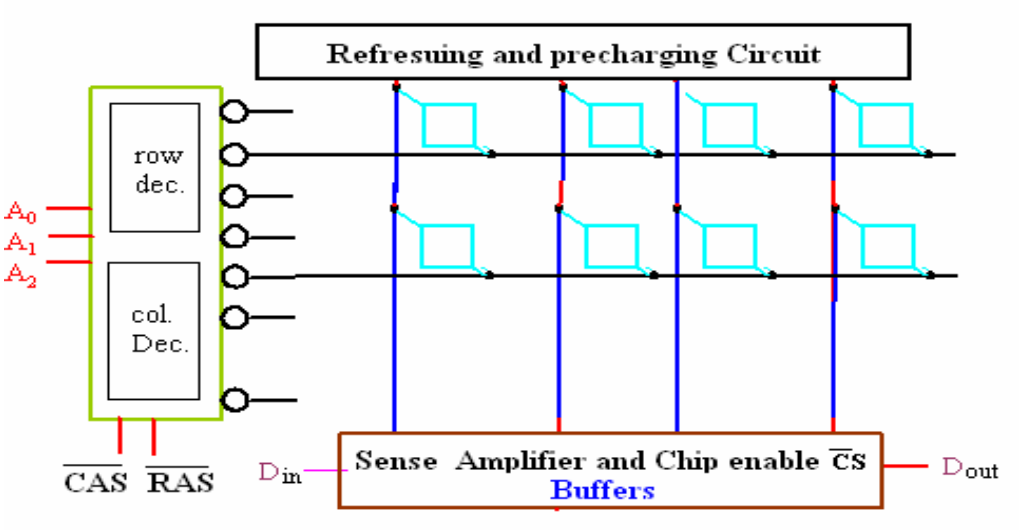


- The remaining two Q's provide access to storage cell and are connected with the address and data busses, as shown in figure

- Sense amplifier is used to find difference of output bit-lines: for negative voltage difference the circuit stores/outputs 'logic 0' and for positive voltage difference the circuit outputs 'logic 1'

Slide 7: **Electronics of Dynamic Read Only Memory (DRAM):**

- DRAM Storage cells, shown as blue boxes, is usually arranged in a square array of one capacitor and transistor per cell.



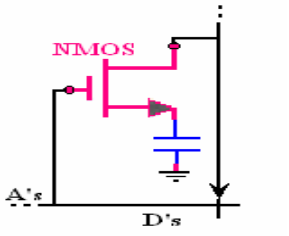
- Although DRAM's provides higher storage density, it requires a more complex read/write mechanism and refreshing circuits.

- The main advantage of DRAM over SRAM is its structural simple storage cells. (*Note: which consist of only one pair of transistor and capacitor, compared to that of SRAM, which consist of 6 transistors*)

Slide 8: **Electronics of DRAM (cont'd):**

- The two dimensional storage of DRAM is accessed using the same address lines, along with either column address strobes ($\overline{CAS}$) or row address strobes ($\overline{RAS}$) signals.

- If a DRAM storage cell (shown) is selected by applying required physical address (A's), the NMOS will allow the capacitors to be charged or discharged to store/write 'logic 1' or 'logic 0', respectively.



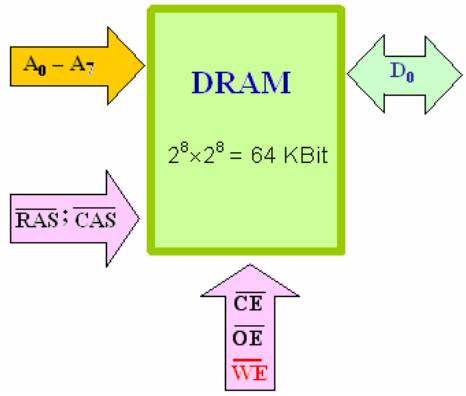
- Once stored, periodic refreshments (≈ in every 3-10 ms) are required to maintain the stored charge and nullify the effects of leakage. This often requires a complicated refreshing circuitry.

Slide 9: **Accessing DRAM Memory Locations:**

The process of accessing the storage in a given DRAM is as follows:

- As the DRAM has 1-bit data bus, each of its storage is bit-wide.

- Thus, 8-bit address bus can access $2^8 \times 2^8 = 64$ Kbit storage locations, organized as an array with individual column (bitlines) and row (wordlines) addresses.



- To read data stored in column-storages locations, we need to apply the 8-bit physical address & $\overline{CAS}$='**0**', $\overline{RAS}$='1', $\overline{WE}$='1'

- But, to write/store data in row-storages-locations, we need to apply the 8-bit physical address, $\overline{CAS}$='1', $\overline{RAS}$='**0**' and $\overline{WE}$='0'

Note: *Remember that the* storage cells in DRAM are capacitive nodes and needs periodically recharging or refreshing to retain stored data.

Slide 10: **CACHE Memory:**

- A computer's system RAM alone is not fast enough to match the speed of the CPU. That is why cache memory is helpful

- Cache is a smaller, faster memory which stores copies of the data from the most frequently used main memory locations.

- During a read/write process, if the CPU interacts with cache memories (instead of RAM), it is known as a “cache hit” and the hit rate measures the effectiveness of this class of memory.

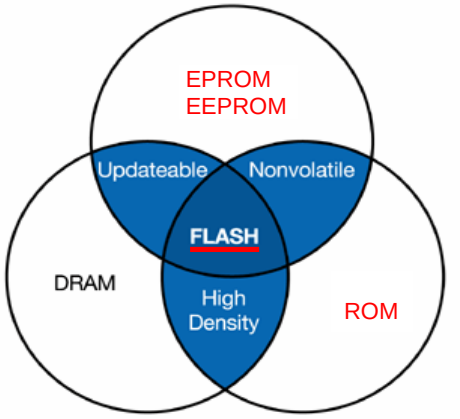
- Popular Cache includes Level-1 cache with capacity of 2 to 64 KB and Level-2 cache with capacity of 256 KB to 2 MB.

Note: ***SRAM is commonly used to implement cache memory.***

Slide 11: **FLASH Memory:**

- FLASH memory is a non-volatile EPROM like memory, where storage cells are erased electrically instead of ultraviolet exposure.

- This solid state devices can be randomly read or programmed as a byte or a word, but must be erased a "block" at a time.



- Like PROM, Flash is also made of a control and a floating gate MOS. In single bit per cell flash, two possible voltage levels exist in each cell, which is controlled by the amount of charge stored or programmed on the floating gate. Depending on a specific threshold voltage of the cell (Vt), the stored voltage levels determine logic storage.

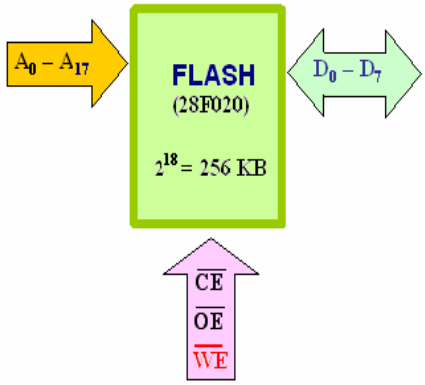
Slide 12: **FLASH Memory (cont'd):**

- Multilevel technology is also used to store **multiple bits** of per cell, to increase the storage density and reduce cost. This is done by assigning a bit pattern to a specific voltage range.

- Typically, this Flash needs 4 second to store 256kB of data (see figure) and 2 seconds for erasure. For the purpose of erasing, these memories are organized in standard array architectures of; bulk-erase, Boot-block and Flash-file.

- Access-time of FLASH is comparable to DRAM and its life cycle allows approximately 100,000 erase/program cycles

- Power-dissipation in FLASH is typically one fifth compared to a similar size DRAM.



Slide 13: **Example 1:**

Question: Tabulate the popular computer storage devices.

Answer:

Computer Storage	
Temporary Storage Areas	Permanent Storage Areas
- CPU Registers - Level 1 and 2 Cache, - Physical and virtual RAM	- ROM, - Magnetic (HD, Floppy, Tape) - Optical (CD, DVD) - Semiconductor (Flash..)

Slide 14: **Example 2:**

Question1:(a) What is the capacity of the DRAM with an address bus of A_0-A_3 and data bus of D_0-D_7.

(b) What is the capacity of a SRAM with same specification?

Answer: (a) DRAM storage locations are organized in an Array, thus total capacity of this DRAM is: $2^4 \times 2^4 = 256$ Byte = 2048 bits.

(b) The capacity of a similar SRAM is: $2^4 = 16$ Byte =128 bits

Question2 : Write some of the features of FLASH memory.

Answer: FLASH memory has the following features: Low cost, High density storage, High speed architecture, Low power and high reliability.